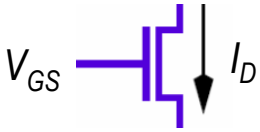
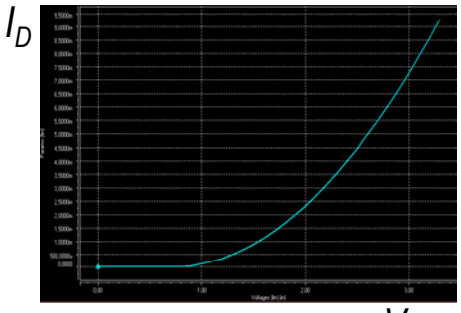
CMOS Scaling Challenges

- Limitation to gate insulator thickness => drain voltage interferes with gate voltage in small channel devices => high I_{OFF}.
  - Multi-gate FETs.
- Fundamental limit in subthreshold slope.
  - Tunnel FETs (Zener commonalities).
  - Impact-ionization FETs (Zener commonalities).
  - Ferroelectric gate FETs.

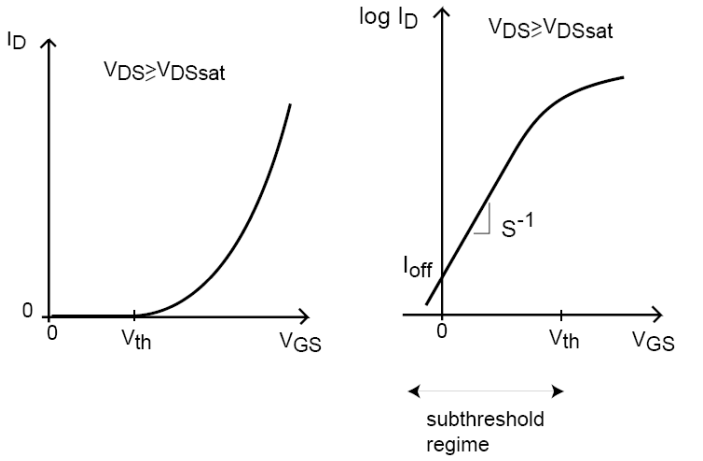
MOSFET Characteristic





$$I_D = \frac{k}{2}(V_{GS} - V_T)^2$$

Subthreshold Operation

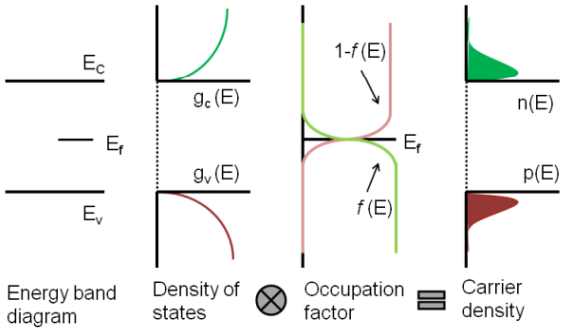


Subthreshold Current

$$I_{ds} = \mu c_{ox} \frac{W}{L_{eff}} e^{1.8} V_{th}^2 e^{\frac{(V_{gs}-V_{T'})}{nV_{th}}} \left(1 - e^{-\frac{V_{ds}}{V_{th}}}\right)$$

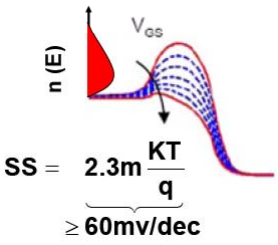
$I_{ds} \propto e^{\frac{(V_{gs}-V_T)}{nV_{th}}}$ when V_{ds} is large $\quad n = 1 + \frac{C_b}{C_g}$

Boltzmann Distribution



- #high energy carriers is exponentially varying with energy level.

Subthreshold Slope (SS)

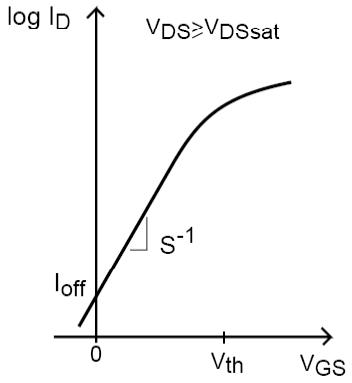


- As gate voltage varies, the carriers available to carry current will vary exponentially.

$$I_{ds} \propto e^{\frac{(V_{gs}-V_T)}{nV_{th}}}$$

$$S = n \cdot V_{th} \cdot \ln 10 = 0.026 \cdot 2.30 = 59.8 \text{ mV/decade}$$

I_{ON} versus I_{OFF}

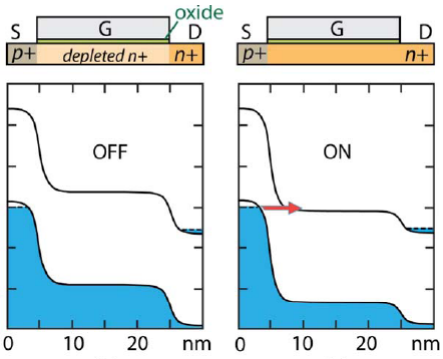


- Decade (10x) of current increase requires 60 mV gate voltage change.
  - Would like more dramatic behavior.
- Why bother?
  - I_{ON}/I_{OFF} ratio important for 1/0.
  - Static power due to I_{OFF}.

Other Devices

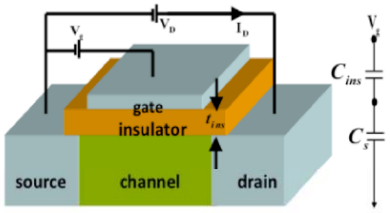
- Improved SS: Tunnel FETs, ferroelectric FETs
  - Nanowire FETs, graphene, …
  - Impact-ionization FETs (I-MOS) have too long delays?
  - Suspended gate FETs (SG-FET).
- Improved SCE: Multi-gate FETs.
  - FinFET.

Tunnel FET



- Low V_{DD} thanks to small bandgaps.
- Carbon NanoTubes, Graphene NanoRibbons

Ferroelectric gate FET



$$n = 1 + \frac{C_b}{C_g}$$

- Make Cb/Cg negative!