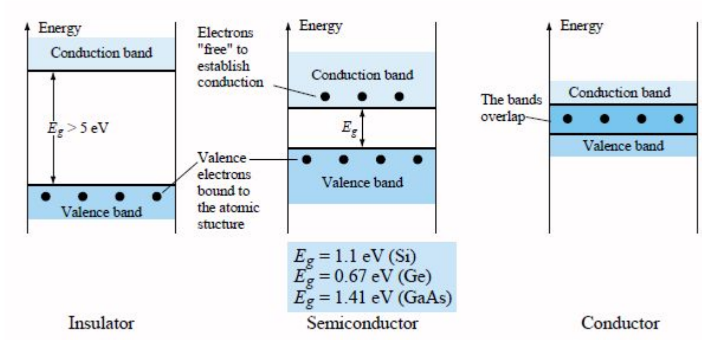
ATV 2011:
Technology Trends in Computer Engineering

Professor Per Larsson-Edefors

Solid-State Devices

www.cse.chalmers.se/~perla/ugrad/SemTech/Lectures_2000.pdf

Semiconductors



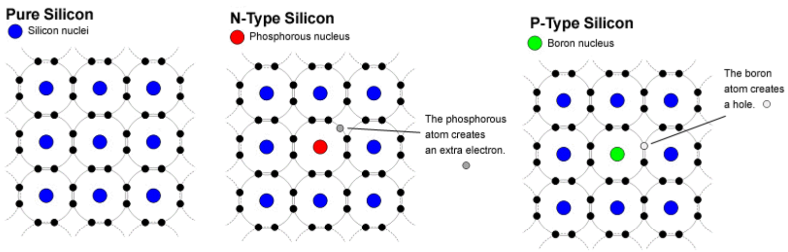
E_g for Si is 1.12 eV
E_g for SiO_2 is 8.9 eV!

1 eV = 1.6 10^{-19} J

Carriers and Temperature

- Semiconductor with no impurities is *intrinsic*. Electrons in valence band may be excited to conduction band, jumping the band gap (#electrons in CB = #holes in VB).
- Si at T = 300 K: 10^{10} free carriers/cm^3. With 2 10^{23} valence electrons/cm^3, less than one bond in 10^{13} is broken.
- #free carriers is an important parameter for semiconductor performance!

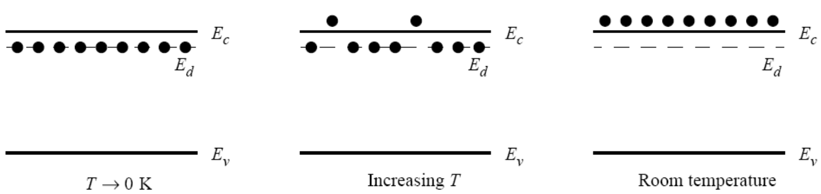
Semiconductor Doping



Silicon (with four electrons in VB) crystal lattice has covalent bonds.

Picture source: Dept. of Physics, Univ Warwick

Free Carriers

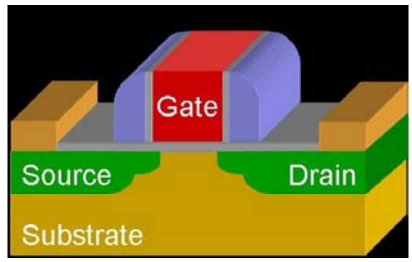


- Intrinsic silicon at T=300K: 10^{10} free carriers/cm^3.
- Using doping (extrinsic semiconductors), carrier concentrations of 10^{15}-10^{18}/cm^3 are possible.
  - Above 10^{18}/cm^3, degeneration happens as E_c-E_d < 3kT. ΔE_g can be as much as 10% of E_g for 10^{19}/cm^3.
- Beside T, voltage and light can excite VB electrons.

MOSFETs and Carriers

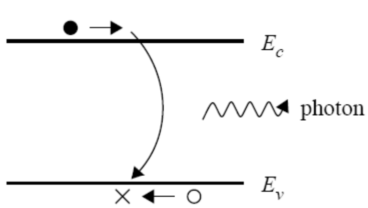
- Definition of threshold voltage, V_T:

  The gate voltage that "inverts" the channel material into one with as many free carriers (electrons/holes) as the doping generated (holes/electrons).



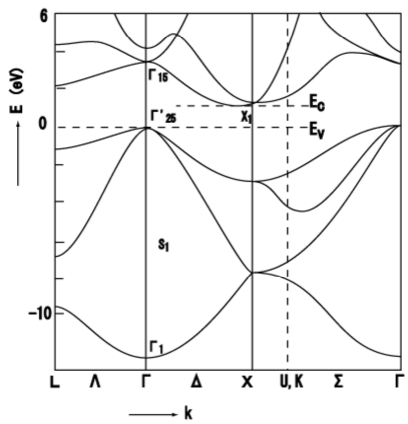
Picture source: USC

Band Gaps for LEDs



- E_g => Planck's constant * frequency of photon (hv).
- Via material innovations, increase band gap to get lower wavelength light.
- First there were red LEDs; then came green, and now blue/white are common.

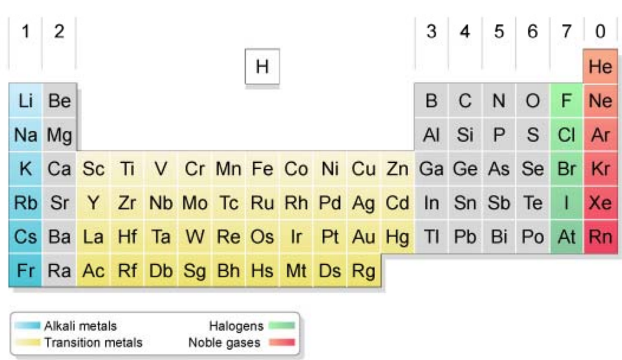
Band Gaps – Solid-State Physics



Picture source: Dept. of Physics, Univ Warwick

- Direct band gaps allow electrons to cross band gap with no change of momentum (k).
- Si, Ge, SiC are indirect.
- GaAs is direct; and a very common constituent of LEDs.

Compound Semiconductors



III/V materials, e.g. GaAs (Gallium Arsenide)

Solid-State Device History

- 1874: Lead-sulfide rectifier by K. F. Braun.
- 1925: MOSFET patent by Lilienfeld.

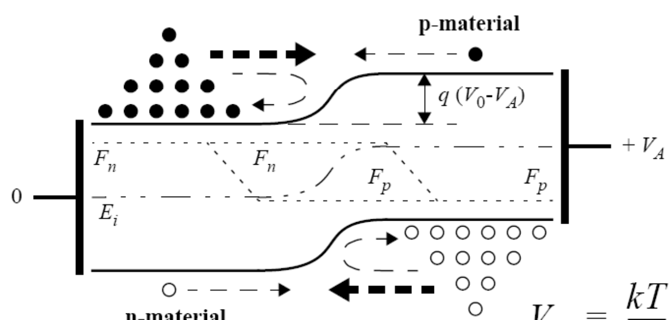
WW2/RADAR development:

- 1937-39: Dopants studied; pn junction (R. Ohl @ Bell).
- 1944: Doping patent (J. R. Woodyard @ Sperry).

Post-WW2 efforts:

- "Bipolar transistor" discovered 1947, Shockley et al.

Forward-Biased Diode

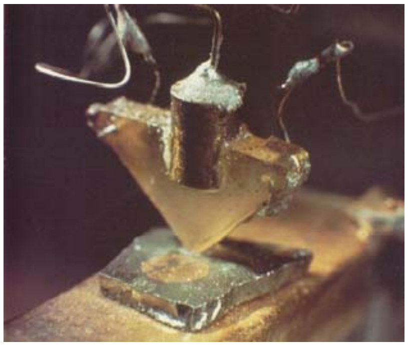


$$V_0 = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^2}\right)$$

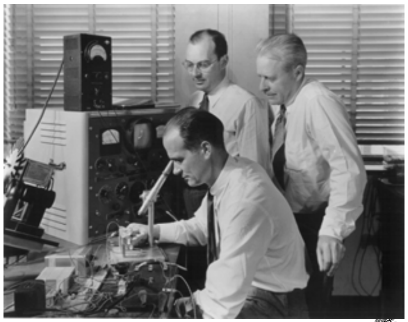
- Diffusion:
  V_A regulates #free carriers that diffuse.

$$J_{t,x} = -J_0\left(e^{\frac{qV_A}{kT}} - 1\right)$$

Dec 16, 1947

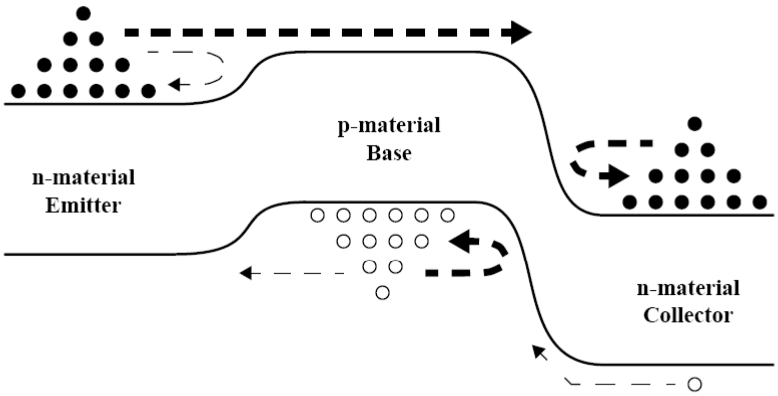


Picture source: TaylorEdge



Picture source: Wired.com

Minority-Carrier Injection

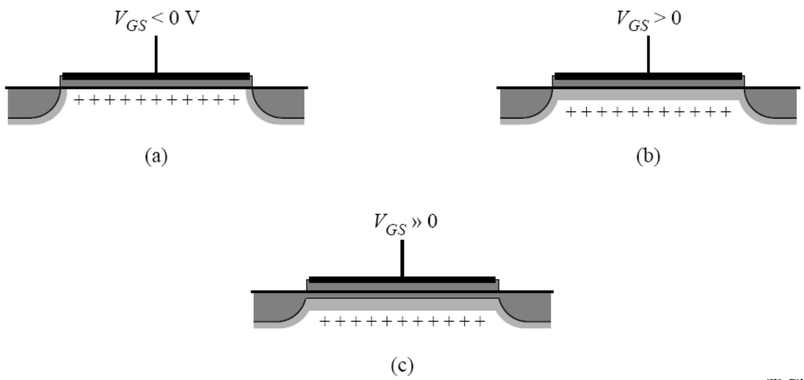


Solid-State Device History, cont.

Further integration (post Sputnik & transistor radio):

- 1958: Hoerni's planar process (Si/SiO_2).
- 1959: Noyce's integrated circuit.
- 1960: Si MOSFET (Kahng and Atalla @ Bell).
- 1966: 1-T DRAM cell (Dennard @ IBM).

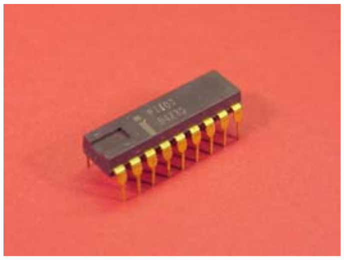
MOSFET Modes



CHALMERS

MOSFET Memories

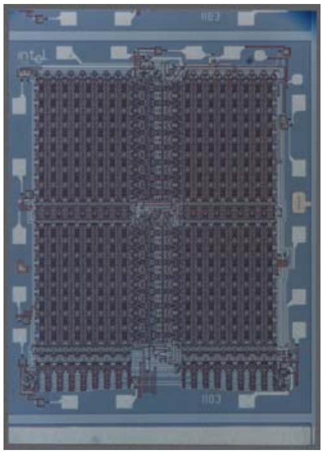
- 1970: Intel 1103, the first DRAM chip (1 kbit, PMOS-based).
- 1972: 1103 becomes the best selling semiconductor memory chip.
- Magnetic core memories are slowly becoming obsolete.
  But in 1976, still 95% of computer memory was magnetic core.



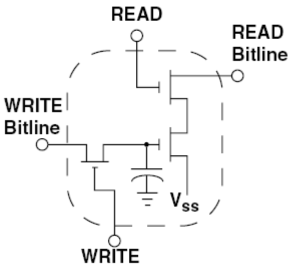
Picture source: Intel

CHALMERS

Intel 1103



Picture source: Intel



Picture source: *Memory Systems*, Elsevier

Multitude of Devices

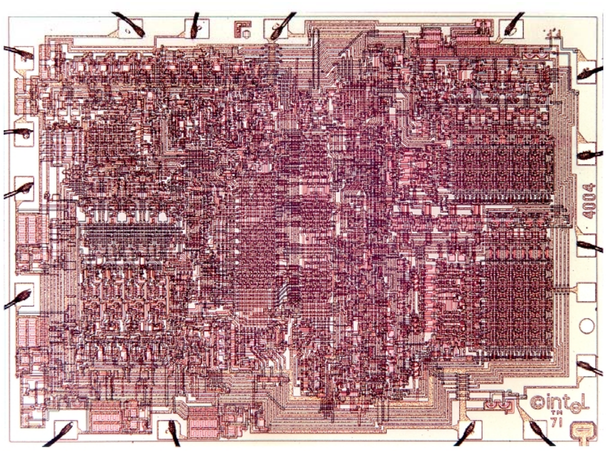
- MOSFETs (IGFETs)
- JFET/MESFET – non-planar techs, e.g. GaAs
- Bipolar
- HBT – high speed analog, InP, SiGe
- HEMT – high speed analog, GaAs/AlGaAs
- “Strained silicon”
- BiCMOS – mixing CMOS and bipolar/HBT

IC Manufacturing

Scaling

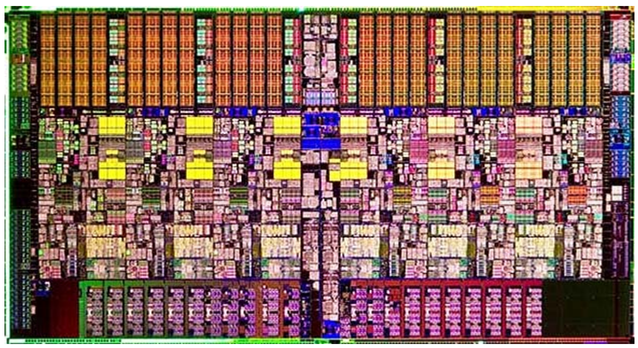
- Technology nodes: referring to lateral dimensions.
  - DRAM (or NAND Flash) m1 half pitch.
- Traditionally lithography-driven scaling.
- Economical limit to lithography-driven scaling (11-15 nm).
- Technology must scale in other "dimensions".
  - Vertical dimension (3D, ILD).
  - New devices.
  - New materials.
    (E-field => VDD: >14 V (PMOS 1103), 12 V (4004))

Intel 4004 – 10 μm



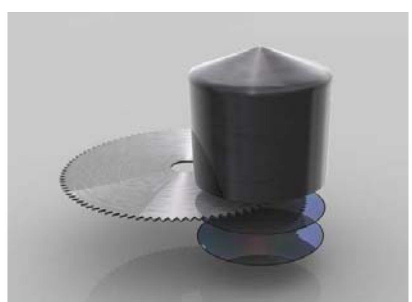
CHALMERS

Intel Core i7 980X – 32 nm

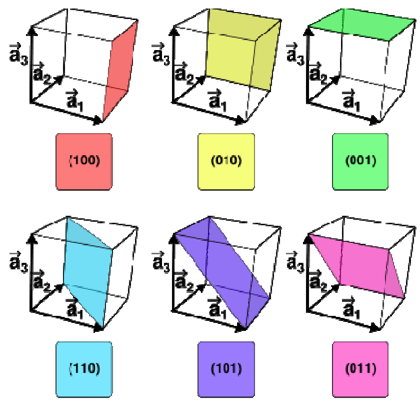


CHALMERS

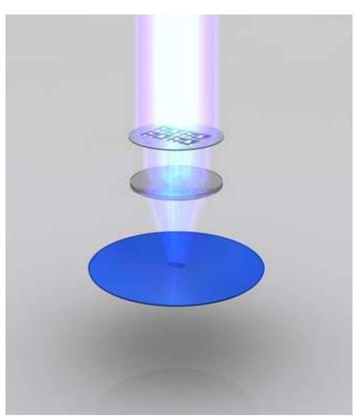
Wafer Production

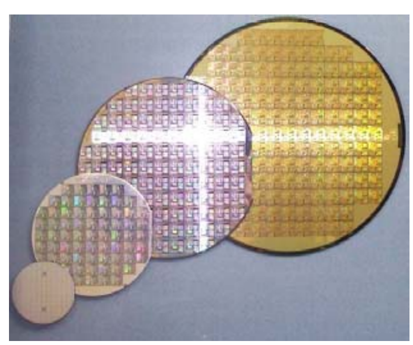


Crystal Orientation Matter



Lithography for IC

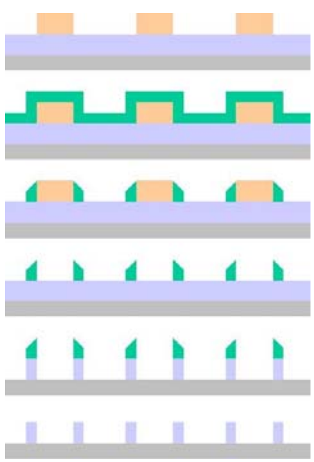




Lithography Challenge

- Speed! Exposure via mask reticle; stepper defines dies.
- Argon fluoride excimer laser at 193-nm wavelength.
  - Absorption edge of air is at 185 nm.
- Optical proximity correction (for increasing #mask layers).
- Numerical apertures exceeding 1.0 possible via immersion in water.
- Double patterning.
- *Future: EUV litho? Light sources? Mirrors? Vacuum? Keep an eye on Intel Fab 42, Chandler, AZ.*

Double Patterning



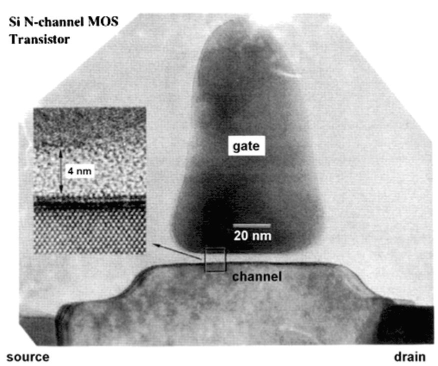
- Line density is an issue.
- Line width is not.
- Double patterning using space walls.

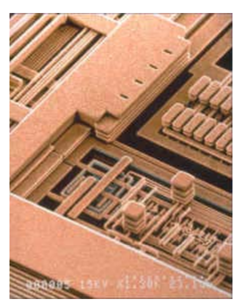
Scaled MOSFETs

- High-k gate dielectric allows electric oxide thickness (EOT) scaling; avoids tunneling. ($C = k\,A/T$, where $k = \varepsilon$).
- Metal gates to avoid gate polydepletion.
  - Work function regulation / V_T tuning difficult.
- Strained (Ge) silicon for mobility enhancement.
  What will happen in multi-gate FETs?

- But … still the MOSFET channel is poorly controlled, leading to substantial subthreshold leakage (and SCE).

Small-Channel Effects (SCEs)





Interconnects

- Performance bottleneck via long RC constants.
  - Lateral dimensions shrink =>
    stack of 10 layers progressively sized.
  - Vertical dimensions cannot shrink as R increases too fast.
- Low-k dielectric for metal stack;
  starting to enter pre-metal layer too.
- All copper layers in processors. Copper bottom layer, with aluminum layers on top in e.g. DRAMs.
- *In view of performance and yield, 3D makes sense…*

ATV 2011

Organization

- September – October 2011.
- 5 cu.
- Several topics:
  - Self study.
    - Initial paper/book.
  - Seminar.

Next Meeting

- Friday Sep 16; 13.30 ?
  - Topic defined (1 page).
    - Expect some help from instructor (away Mon-Wed).
    - No significant topic overlaps allowed.
  - Bring calendar; more meetings scheduled.
- **www.cse.chalmers.se/~perla/grad/ATV/**
- You have to make yourself known;
  email me name and “personnummer”.

Topics – Study + Seminar

- Alen - 3D chip integration
- Angelos - Volatile 3D memory technologies
- Dmitry - Non-volatile memory technologies
- Kasyab - Memristor technology
- Erik - On-chip optical interconnects
- Tung – FinFETs
- Anurag - 14 nm fabrication