FlexSoC

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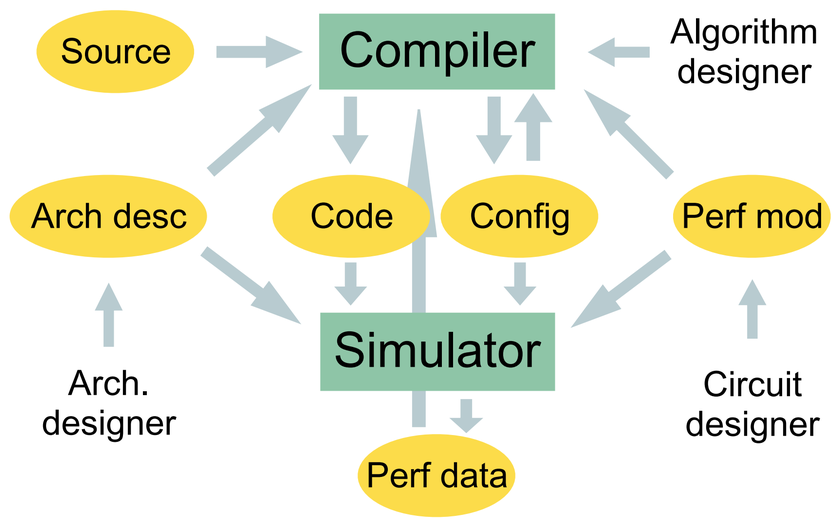
Background

The FlexSoC program, launched during 2003, aims to develop new architectural techniques for the complex processors necessary for high-performance embedded systems. One of our driving examples is the high-performance cellular phone. Many present-day cellular phones have features (such as games, 3d graphics, video playback, and wireless Internet connectivity) which until recently were only available in high-performance desktop computers. Moreover, in the cell-phone case, these features must be delivered in a package small enough to fit a purse or a pocket, and at fractions of the price and power dissipation of a desktop system.

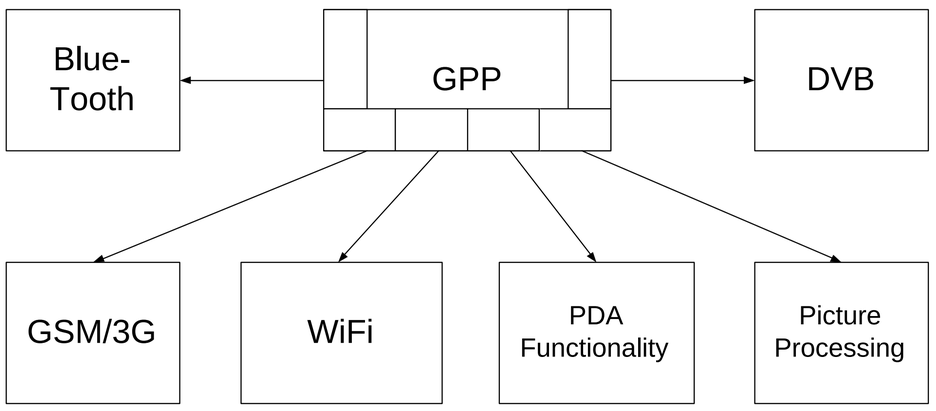
The power dissipation is an especially vexing problem for a cellular phone. A high dissipation has many undesired consequences: batteries drain too quickly, or must otherwise be large and heavy; elaborate and costly heat-removal arrangements must be employed; and reliability is also adversely affected. Finally, the environmental load of consumer-electronics products is dominated by the power used in the field, so lower dissipation makes a product more environmentally friendly.



Simulator and evaluation framework

Motivation

- System on the Chip solutions are commonly based around a General Purpose Processor that coordinates the computation of the different hardware accelerators by controlling them using special purpose device drivers
- This design methodology leads to a complicated heterogeneous programming interface with an Add-Hoc nature of both control and synchronization
- The hardware accelerators are hardwired for a specific application making it difficult to adopt the architecture to new standards of evolving protocols



Traditional heterogeneous SoC

Benefits

The FlexSoC framework will contribute to the ease of development of future System on Chips and shorten the time to market that is becoming ever more crucial to be competitive for companies in the digital manufacturing business.

The benefits with FlexSoC will be

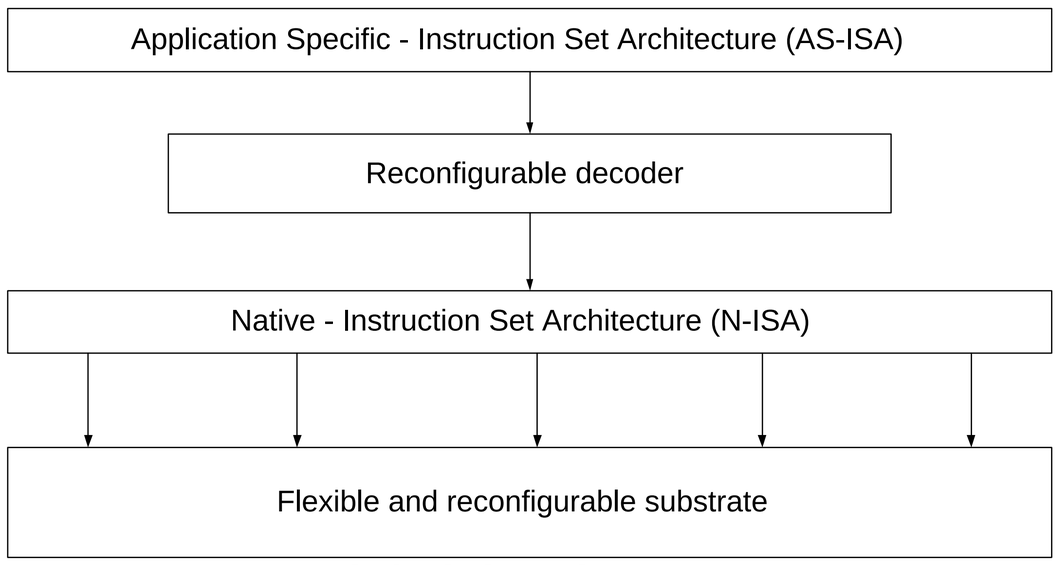
- Common programming interface
- Reconfigurable/flexible datapaths
- Synchronization framework
- Power and performance framework
- Power- and performance-aware compiler

More Info

For more information visit our homepage at:
http://www.cs.chalmers.se/~flexsoc/

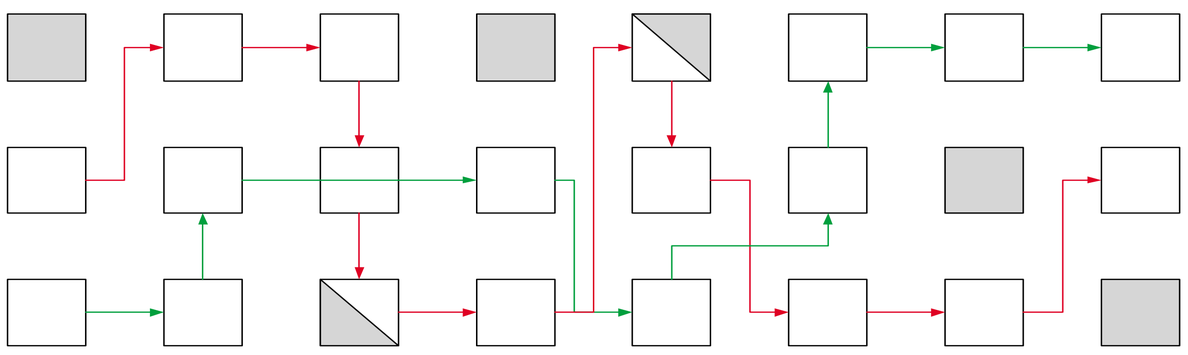
Ideas

- The FlexSoC concept is built on the existence of a Native ISA (N-ISA) that controls the whole chip
- In order to reduce the instruction bandwidth and instruction word size an Application Specific ISA (AS-ISA) is constructed from the N-ISA
- The translation from AS-ISA to N-ISA is done on-chip and in real-time
- The translation will be reconfigurable in order to be able to support different AS-ISA's



FlexSoC AS-ISA/N-ISA approach

- The substrate that the N-ISA is controlling is viewed as a sea of Functional Units (FU's)
- A FU is a pure function, a memory, or a combination of these with a simple uninterruptable computation
- Any FU can communicate with any other FU but a cost, known to the compiler, is associated corresponding to the distance between the communicating FU's
- The routing between the FU's are reconfigurable as well as some of the FU's themselves making it possible to create application specific datapaths
- The inherent nature of System on Chips with simultaneous execution of multiple threads has to be supported by the underlying hierarchical control structure



Reconfigurable datapaths in FlexSoC