A practically oriented study guide to help prepare for the written exam in Hardware Description and Verification

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1. Look at the exam for 2009 and the brief answers at
   `http://www.cse.chalmers.se/edu/course/TDA956/OldExams/`
   The exam for 2011 will have a similar shape, though will maybe be slightly harder :)
   (I did not set the 2009 exam.)

2. Revise the writing of PSL specs about very small circuits. This might be best done by concocting or finding some very small circuits and making up specs about them (and checking them). As well as looking at the above Solutions09 file, review the PSL lab and t.h. exam just to remind yourself about PSL, VHDL and testbench writing (but I will not ask technical questions directly about the lab or t.h. exam). However, be prepared to discuss *your view* of PSL-based verification.

3. Review BDDs and make sure that you can correctly construcct an OBDD from a small formula, *showing all the steps*.

4. Review the use of formulas and/or BDDs to represent sets of states and transition relations in model checking.

5. Review the ideas of bounded model checking and temporal induction. Be able to write down formulas or programs to define them. Probably the most efficient way to do this is to look at Sections III and IV of the "SAT-solving in practice" paper (see Schedule). I will not ask exam questions about how SAT-solving itself is done.

6. You should be able to write down small CTL formulas for simple English specifications (like the examples in the lectures).

7. For CTL model checking, you need to be able to do a fixed point iteration like the one shown in the answers for 2009.

   Thomas Hallgren's little model checker might help with this, although it is very important to practise the kind of *manual* calculation that is shown in the above

solution file, and in the Carl Seger paper on the Schedule. The model checker can help you to check your answers. See
`http://www.cse.chalmers.se/edu/course/TDA956/TH/MC/`
In testmc.hs, Thomas shows how to use his MC on the example that I used in the lectures about CTL MC. In
`http://www.cse.chalmers.se/edu/course/TDA956/OldExams/Circuit2MC.hs`
I do the same thing for the Circuit2 example from the above exam paper. [Note: The answer shown for Question 3.2 in the above Solutions for 2009 shows an xor in the equation for y', where I expect a nor (the inv of or). See
`http://www.cse.chalmers.se/edu/course/TDA956/OldExams/Circuit2.hs`
which confirms that putting xor there is not correct. Note that the transitions shown in the Solutions and the fixed point iteration are correct, as can be checked using the little model checker program.]

8. The above Solutions file contains (for Question 4) a small Lava property about circuit2. I have copied this to the Circuit2.hs file so that you can play with it. Look also at the Lava tutorial, sections 6.1 and 6.2 and at some of the exercises for that chapter. In our use of Lava (as covered in the course) we don't use induction (section 6.3) but rely on SMV for sequential verification. In addition to these kinds of very small circuits and properties, make sure you know how to verify properties of generic circuits using Lava (fixing the input size). You have done plenty of this in the Lava Lab and Take Home Exam, though.

9. There are probably other topics that I have forgotten to mention. I don't guarantee that the above list is exhaustive. But if you know all this and have worked hard on the labs and t.h. exams, you will do fine!

10. Although I am keen for you to know about the current state of formal verification in industry, and this is why I provided the IBM paper by Paruthi on the Schedule and other materials on the Links page, I will not ask exam questions about this. For your longer term learning, I advise reading some of these materials :)

Please mail Mary if you have any questions. Good luck!