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Integrating Design and Verification — From Simple Idea to Practical System

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Abstract

For many VLSI designs, validation has started to dominates the total design effort. In addition, historical trends are indicating that this problem will continue to grow. For example, data from Intel's lead microprocessor design efforts shows that the number of pre-silicon bugs has increased by a factor of four for every lead project for the last 25 years. If this trend is not broken, Intel's next lead design is likely to have to go through the "find the bug, evaluate it, root cause it, fix it, and validate the fix" process tens of thousands of times; potentially overwhelming the validation and design team. Thus one of the most critical goals for improving the design process is to break this bug trend.

In the presentation, we introduce the Integrated Design and Verification (IDV) system that has been developed at Intel for the last 5 years. IDV combines the design and validation efforts so that the task of design validation (i.e., "Did we capture what we actually wanted?") is significantly simplified by means of a much smaller and much more stable high-level model. Furthermore, when the design is completed, so also is the implementation validation (i.e., "Did we implement what we intended?"). The latter is accomplished by linking the design process very tightly with the validation process. Although this idea is not new, the combination of correct-by-construction and correct-by-verification and the tight integration of a database of verified results is new and has led to a design environment that allows rapid design in which the validation problem has been significantly reduced.

To make the presentation more realistic, we will use the design, from a high-level model to layout, of a floating point execution unit as a driving example. We will discuss the early design phase in which the high-level model is refined using algorithmic transformations to a viable micro architecture; continue with the middle level design in which the actual logic implementation is derived and conclude with the final placement and layout stage. Although the design process conceptually is performed sequentially, we will illustrate the tight loop that IDV enables between physical design and logical/micro-architectural design. The latter is a critical component in enabling design convergence. In fact, in today's process technology, integration of physical and logical design is not optional but rather mandatory.

Dr. Carl Seger *received his B.Sc and M.Sc. in Engineering Physics from Chalmers' University of Technology, Sweden in 1985 and his M.Math and Ph.D. degrees in Computer Science from University of Waterloo, Canada, in 1986 and 1988 respectively. After an academic career at Carnegie Mellon and the University of British Columbia, ending as Associate Professor, he joined Intel at the end of 1995 and is now a Senior Principal Engineer in Design Technology's Strategic CAD Labs. He is the author of the Voss (a.k.a. Forte) formal verification system, that forms the basis of almost all formal verification tools in Intel, and has published over 40 papers and books and holds 4 patents. More recently he developed the concepts behind the Integrated Design and Verification system and implemented much of the fist version of the system.*

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