Jasper Overview

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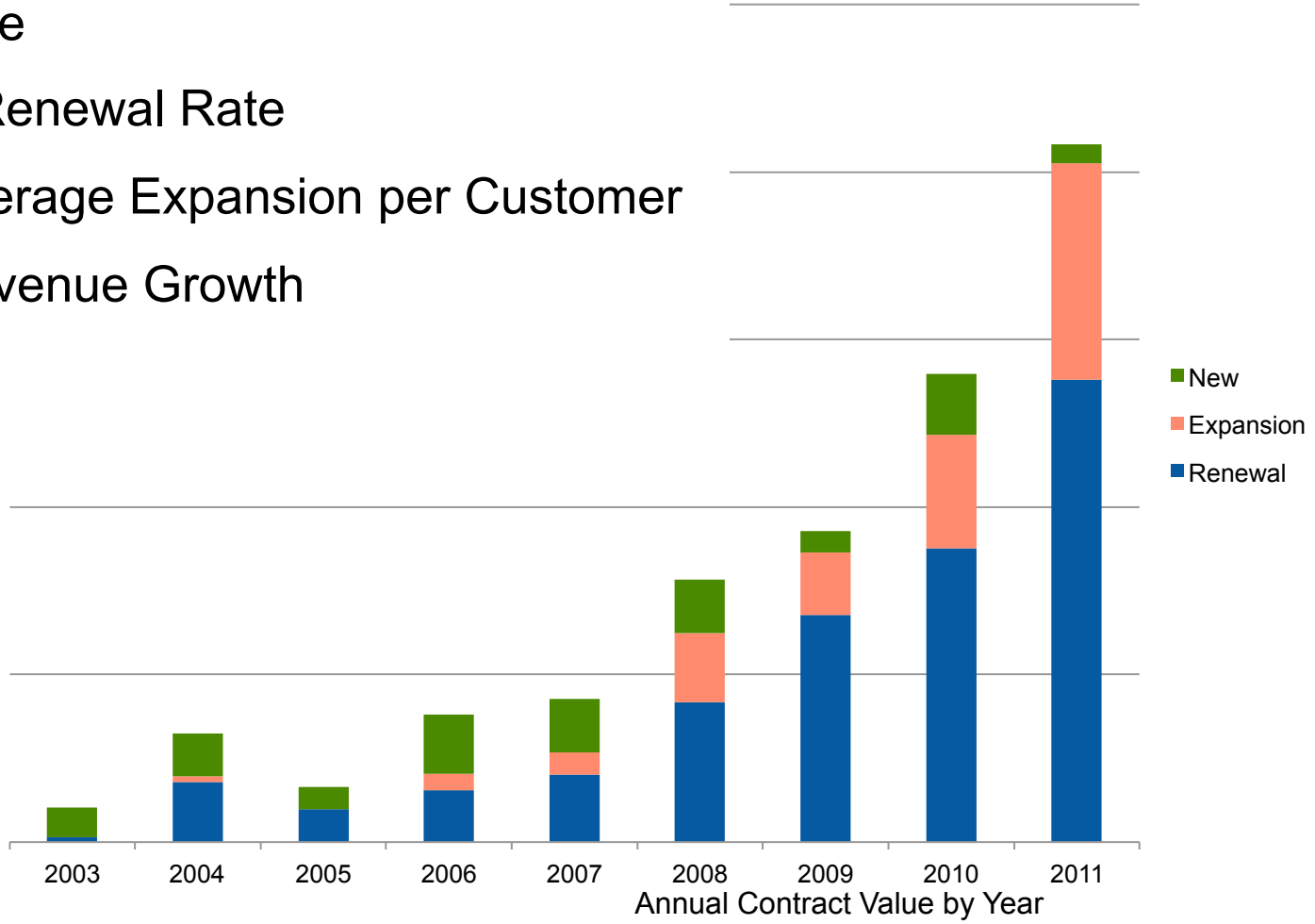
About Jasper

- Jasper Design Automation
  - We are the leading provider of SoC design and verification solutions leveraging advanced formal technologies
- Jasper Users
  - Our customers include system architects, logic designers, verification engineers, and silicon bring-up teams
- Jasper's Success
  - Our year-to-year exponential growth based on successful, proven technologies; excellent AE support; and deployment-driven business model

Strong Financial Results in 2011

- Profitable
- 98.5% Renewal Rate
- 66% Average Expansion per Customer
- 69% Revenue Growth



Market Share Growth

Market Statistics Service | **2011 ● Second Quarter Report**

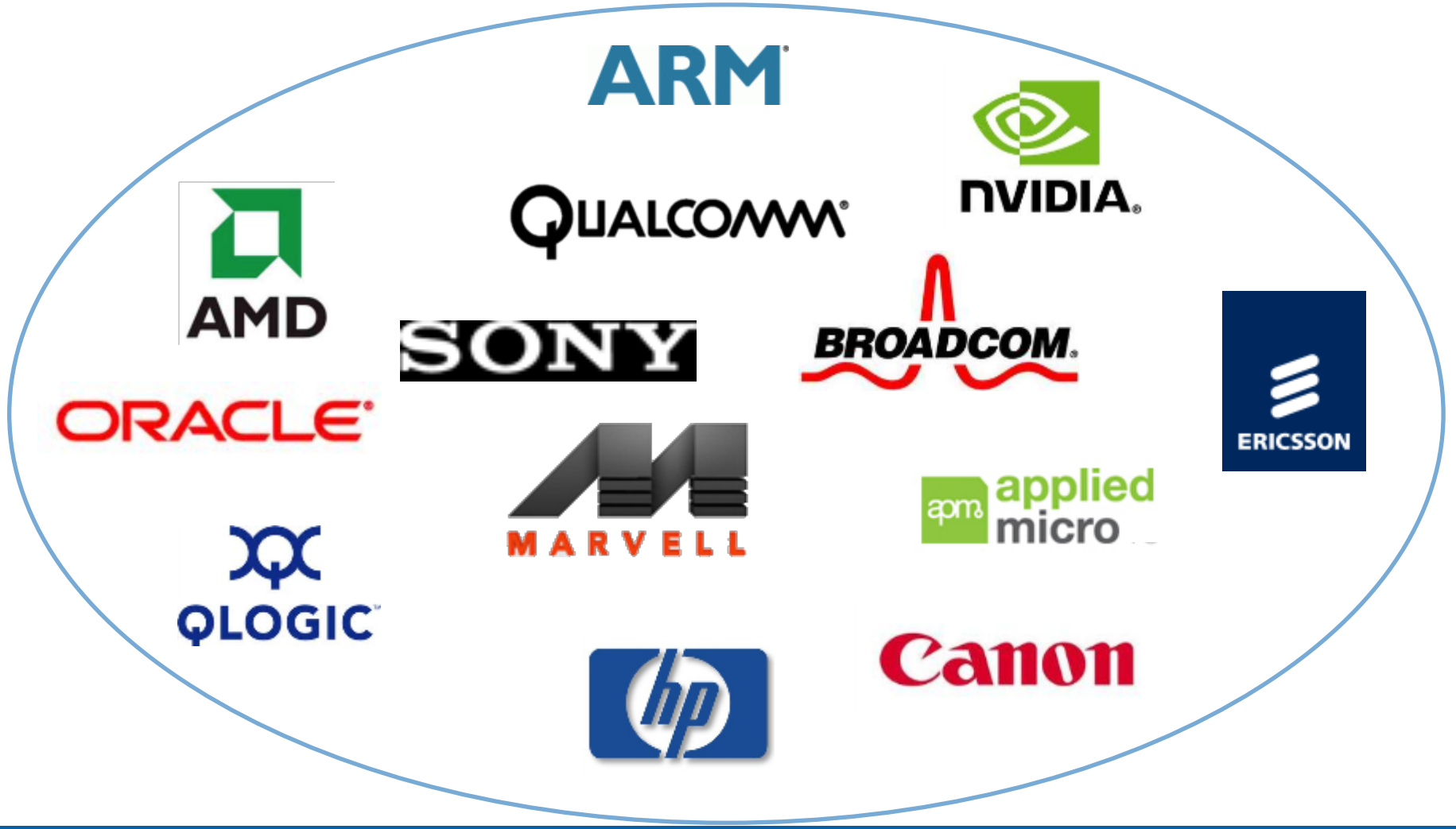
***CAE Worldwide Revenue by Quarter** ($Millions)*

	2008				2009				2010				2011			
CAE (continued from previous page)	**Q1 †**	**Q2 †**	**Q3**	**Q4**	**Q1**	**Q2**	**Q3**	**Q4**	**Q1**	**Q2**	**Q3**	**Q4**	**Q1**	**Q2**	**Q3**	**Q4**
2.5 Formal Verification	**24.4**	**22.2**	**19.0**	**23.1**	**19.4**	**21.0**	**24.4**	**22.0**	**22.1**	**25.1**	**28.5**	**33.1**	**32.2**	**28.3**		
2.5.1 Equivalency Checking	18.0	16.7	12.7	16.9	13.8	15.0	17.0	13.8	13.7	15.7	16.3	19.1	17.3	16.4		
2.5.2 Property Checking	6.4	5.5	6.4	6.3	5.6	6.0	7.4	8.2	8.4	9.4	12.1	14.0	14.9	11.9		

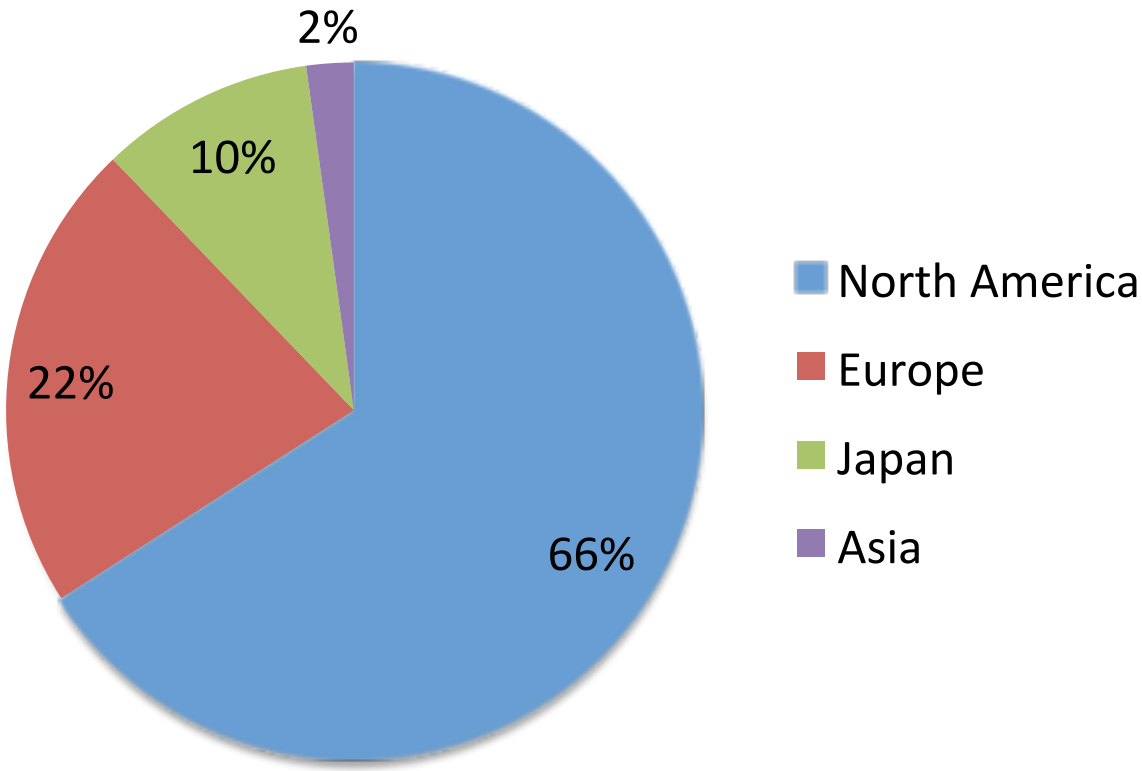
According to EDA Consortium Market Statistics Service:

- With five vendors reporting, Jasper commands 34% of the Formal Property Verification market and has gained market share in the past year
- Jasper revenue is growing 20% faster per year than the overall market

Partial Customer List



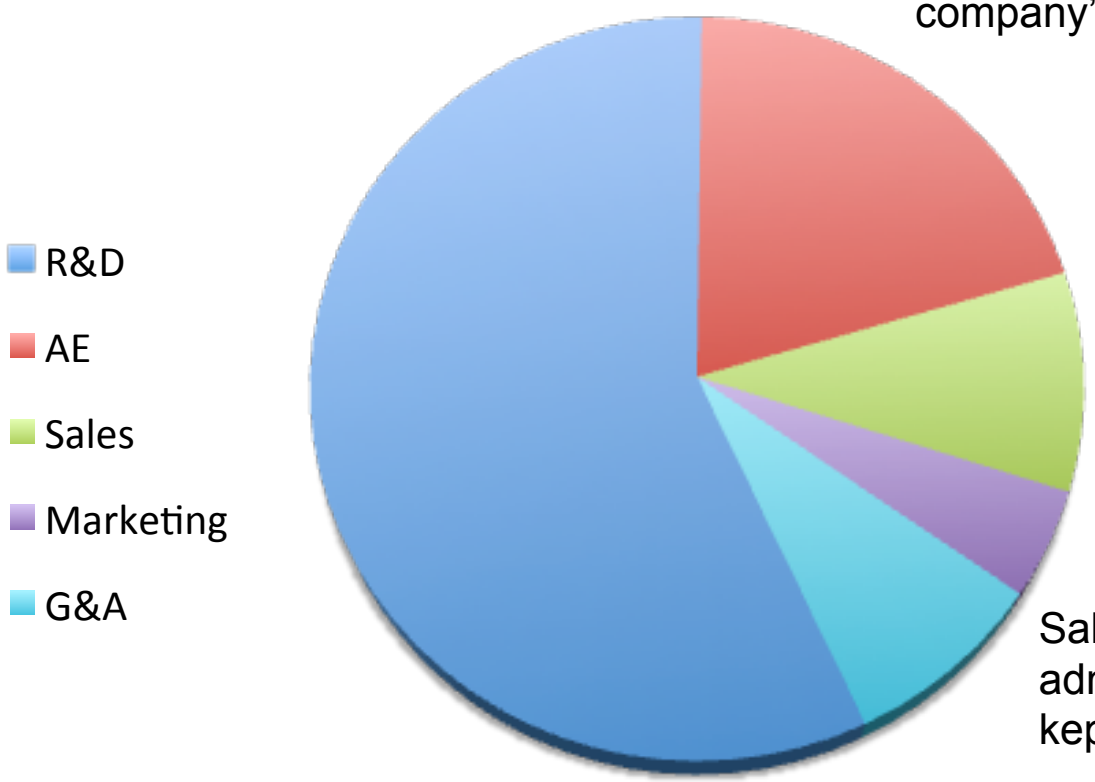
Business by Geographical Region



Jasper Headcount Distribution

High level of R&D investment enables continuous delivery of breakthrough solutions

Application engineering (AE) activities must generate sufficient revenue to fund the company's operations



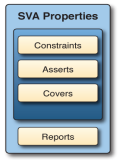
Sales, marketing, and administrative headcount is kept to a minimum

Jasper R&D Centers

- Development sites in US / Sweden / Brazil / Israel
- ~60 engineers
- ~15 PhD in Formal Verification

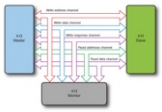
Jasper Product Update

A Wide Range of Applications



Property Synthesis (Structural / Behavioral)

- Automated assertion generation
- Functional pre-defined property generation
- Inference & synthesis of properties from RTL & simulation
- Identification of coverage holes



Intelligent Proof Kits and Verification IPs

- Certification of AMBA 4/ACE checkers
- Popular standard protocols
- Configurable, illustrative, optimized for formal

Formal Property Verification

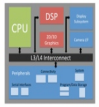
- Protocol certification
- End-to-end packet integrity
- Asynchronous clocking effects
- Assertion-based verification
- Proofs for critical functionalities
- Debug isolation and fix validation

Executable Spec

- Design IP documentation
- Cross references among document, waveform, and RTL
- Configurable waveforms

RTL Development

- Waveform generation from intent
- Designer-based verification w/o testbench
- Design trade-off analysis



Connectivity Verification

- Chip-level connectivity
- Conditional connection with latency

X-Propagation Verification

- Unexpected X: Detection and debug

CSR Verification

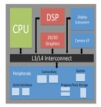
- Automated register verification

Architectural Modeling

- Executable spec
- Absence of deadlock
- Cache coherency

Post-Silicon Debug

- Failure signature matching
- Root cause isolation
- Candidate cause elimination
- Validation of fixes before re-spin



Other SoC related Applications

- Glitch detection
- Multi-cycle path verification

Higher Capacity
Verify complex 100M gate designs

Interactive Debug
Modify/create properties on the fly to explore design behavior

Increased Throughput
Utilize multiple proof engines on parallel compute resources

Wider Deployment
Proliferate across engineering teams with unique adoption model

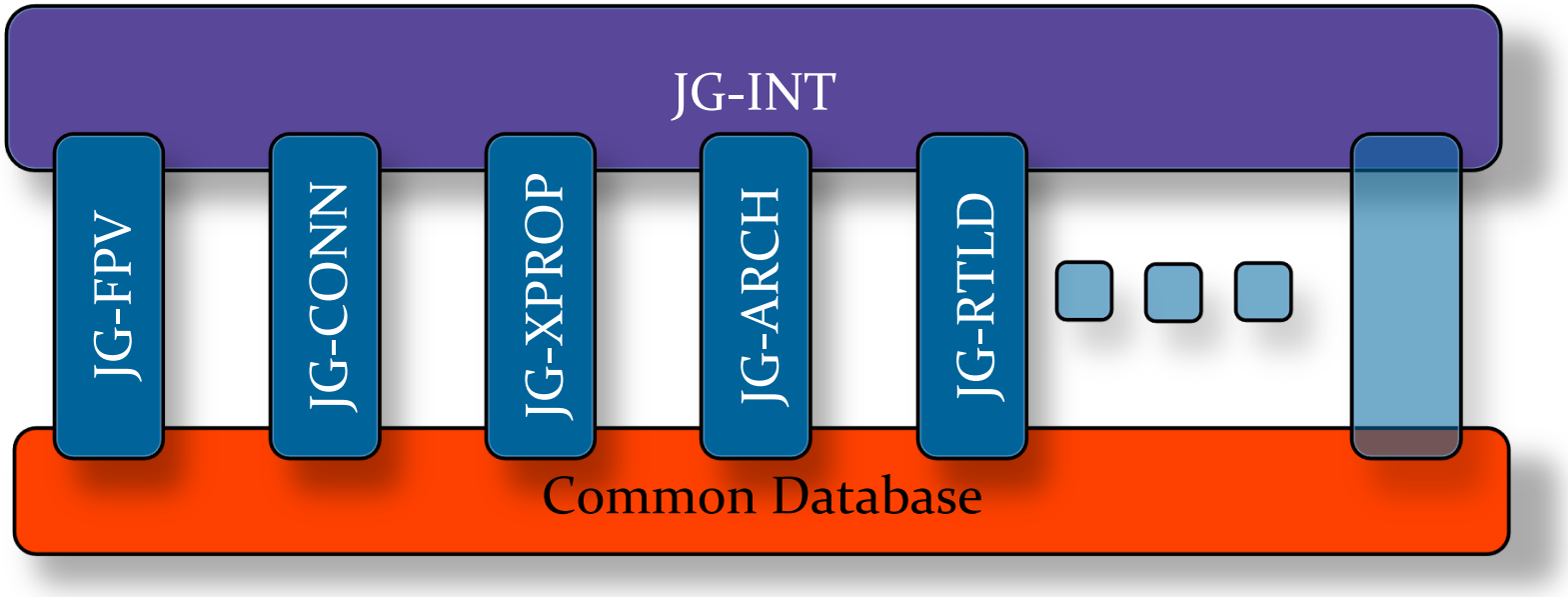
Synergy
Leverage results from one App in other Apps with common GUI/DB

Jasper Products and Solutions

- JasperGold® APPs
  - JasperGold-INT
  - JasperGold FPV: Formal Property Verification
  - JasperGold CONN: Connectivity Verification
  - JasperGold X-PROP: ‘X’ Propagation Verification
  - JasperGold RTLD: RTL Design Verification
  - JasperGold ARCH: Architectural Modeling
- ActiveProp™: Property Synthesis
- Post-Silicon Debug
- Intelligent Proof Kits

JasperGold Apps: Architecture

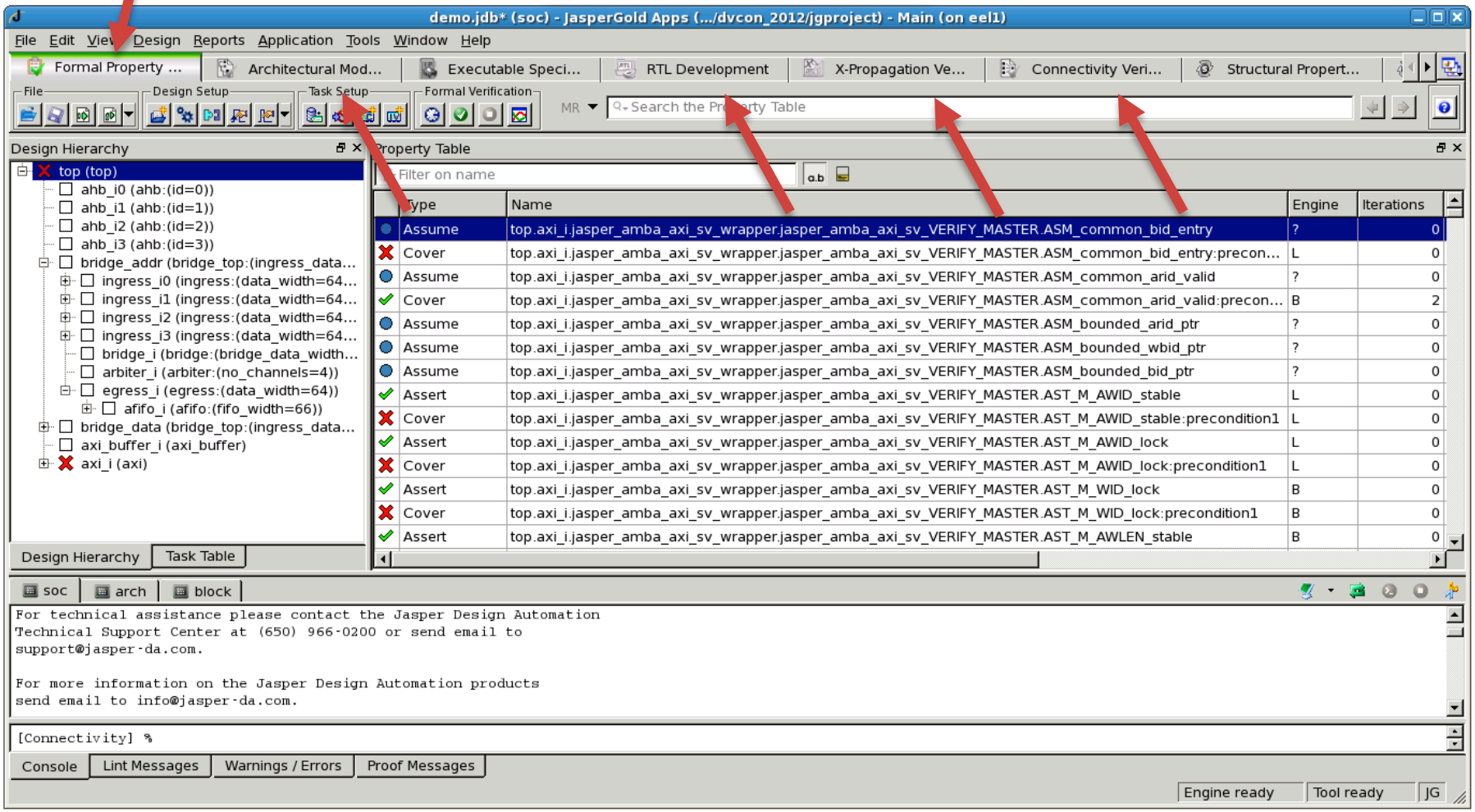
- Innovative platform for proliferating formal verification flows
- Single GUI for all Apps
- Common database enabling cross-App leverage
- Extensible architecture for future Apps



Motivation for JasperGold Apps

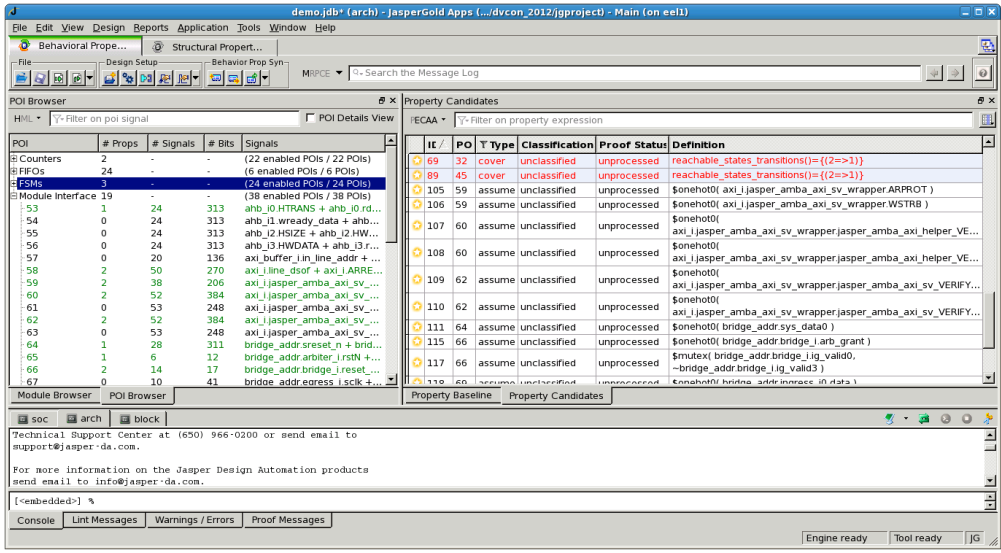
- Promote available flows to users through well-packaged solutions
- Enable a project to run multiple applications on the same block
  - Share work product among applications through a common database
  - Reduce total effort for the project
- Enable a user to run multiple applications on the same block
  - Encourage parallel usage of applications through a common interface
  - Simplify interaction between applications for seamless experience
- Enable a user to harness the power of the server farm
  - Launch parallel jobs from any application through a common interface
  - Collect results from parallel jobs into a common database
- Enable flexible deployments of applications
  - Provide customers affordable access to multi-license use for specific applications
  - Allow Jasper to introduce and grow applications in a systematic way

JasperGold® Apps



ActiveProp™

- Jump-start and automate assertion creation: Generate standard SVA
  - Expand verification property set with intelligent properties
- Increase functional coverage with unique multi-cycle analysis and hierarchy support
- Structural Properties:
  - Extracted from RTL
  - No testbench required
  - Valuable during RTL development
- Behavioral Properties:
  - Extracted from simulation (with/without knowledge of RTL)
  - Quality of properties directly tied to maturity and quality of the simulation results
  - Usually used in later stages of verification

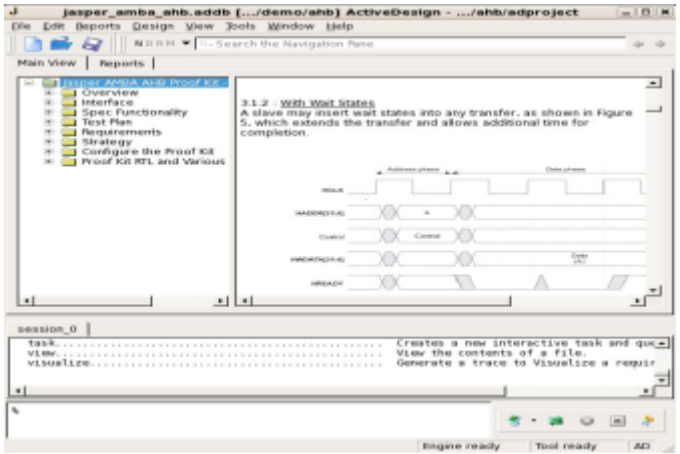


Formal for Post-Silicon Debugging

- Failure signature matching
  - Reproduce failing scenario in the lab
- Root-cause isolation
  - Formal will find ways to falsify the same assertions if the fix does not fix the root cause
- Candidate-cause elimination
  - Accurately eliminate false candidate blocks and scenarios
- Validation of fixes before re-spin
  - Exhaustively verify that fix does not introduce new bugs

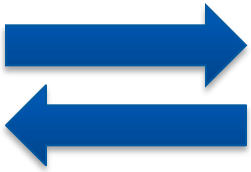
Intelligent Proof Kits

- Properties to verify standard bus and memory controller protocols
  - Standard Interfaces (OCP, AMBA4/AXI, etc.), memory controllers (DDR3, LPDDR2, DFI, etc.)
- Accelerate protocol certification
  - User configurability for variants on standard protocols
  - Early exploration and verification of protocol specification
  - Optimized for formal verification
  - Simulation-friendly properties

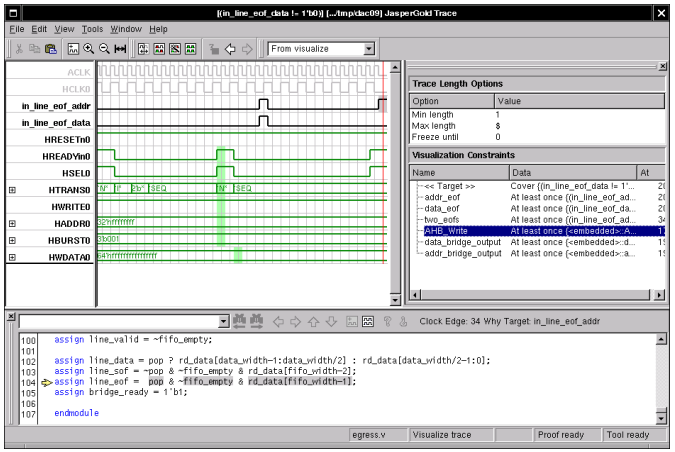


Executable protocol spec

Bring-up and customize waveform



Point to relevant section of spec



Jasper Visualize