Dependability Analysis of Two Candidate Architectures for a Brake-By-Wire System

Laboratory report in

EDA122 Fault-Tolerant Computer Systems

{Author 1}

{Author 2}

Group Number:

Chalmers University of Technology

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# Introduction

{This section shall introduce the reader to the subject addressed by the report. It should include i) a brief explanation of how a brake-by-wire system works and its main advantages and drawbacks compared to existing brake systems, and ii) a description of the purpose of the report, i.e., a formulation of the problem to which the report provides an answer. The last paragraph should consist of a “roadmap” of the report.}

SB1

SB2

WU

WU

Figure 1: Brake-by-wire system

CU

WU

WU

Brake pedal

# Overview of candidate architectures

{This section shall describe the centralized and distributed architectures, and the two modes of operation (full functionality and degraded functionality). It should also describe the modelling assumptions, including the model parameters.}

## Centralized Architecture

{text}

## Distributed Architecture

{text}

## Modes of Operation

In this section you describe the two modes of operation of the system; *full functionality* and*degraded functionality*.

### Full functionality

{text}

### Degraded functionality

{text}

## Assumptions and modeling parameters

{text}

Table 1: Failure rates and coverage factors for the distributed architecture

|  |  |  |  |
| --- | --- | --- | --- |
| **Subsystem** | **Part** | **Failure rate (****)** | **Coverage** |
| System bus | Serial bus | 5•10-7 [f/h] | 1 |
| Wheel unit | Computer module | 15•10-6 [f/h] | 1 |
|  | Sensor | 2•10-6 [f/h] | 1 |
|  | Actuator | 1•10-6 [f/h] | 1 |
| Central unit | Computer module | 8•10-6 [f/h] | 0.99 |

Table 2: Failure rates and coverage factors for the Centralized Architecture

|  |  |  |  |
| --- | --- | --- | --- |
| **Subsystem** | **Part** | **Failure rate (****)** | **Coverage** |
| System bus | Serial bus | 5•10-7 [f/h] | 1 |
| Wheel unit | Computer module | 10•10-6 [f/h] | 1 |
|  | Sensor | 2•10-6 [f/h] | 1 |
|  | Actuator | 1•10-6 [f/h] | 1 |
| Central unit | Computer modules | 10•10-6 [f/h] | First CM failure:1  Second CM failure: 0.99 |

# Description of Models

{This section shall describe your models for the different subsystems for the two architectures and the two levels of functionality. Figures should be explained in the text.}

## Wheel Unit Model

CM

BI

SB1

SB2

Figure 2: Wheel unit

CM

Figure 3. Reliability block diagram of the wheel unit

## Wheel Unit Subsystem Model

{text}

Figure 4: Fault tree for the Wheel Unit Subsystem, full functionality

**WU**

**≥ 1**

**WU**

**WU**

**WU**

Figure 5: Fault tree for the Wheel Unit Subsystem, degraded functionality

## Central unit (CU)

### Distributed Duplex Architecture

CM

BI

SB1

SB2

CM

Figure 6: Central Unit, duplex configuration

Figure 7: Reliability block diagram for the Central Unit, duplex configuration

**A**

**B**

**C**

Figure 8: Markov model for the Central Unit. duplex configuration

### Centralized Triplex Architecture

CM

SB1

SB2

CM

CM

Figure 9: Central Unit, triplex configuration

{Reliability block diagram for …, Figure 10. Make sure the caption number is correct.}

{Markov model for …, Figure 11.}

## System Model

### Centralized Architecture

{Fault tree for Full Functionality, Figure 12.}

{Fault tree for Degraded Functionality, Figure 13.}

### Distributed Architecture

{Fault tree for Full Functionality, Figure 14.}

{Fault tree for Degraded Functionality, Figure 15.}

# Results

{Describe the results. Graphs and tables shall be commented in text. To facilitate the comparison of the results for different design solutions, include several reliability graphs in one diagram.}

Table 3: Reliability and MTTF results

|  |  |  |
| --- | --- | --- |
| **Units** | **Distributed** | **Centralized** |
| ***Wheel Unit*** | R=  MTTF= | R=  MTTF= |
| ***Wheel Unit Subsystem Full Functionality*** | R=  MTTF= | R=  MTTF= |
| ***Wheel Unit Subsystem Degraded Functionality*** | R=  MTTF= | R=  MTTF= |
| ***Central Unit*** | R=  MTTF= | R=  MTTF= |
| ***Entire System Full Functionality*** | R=  MTTF= | R=  MTTF= |
| ***Entire System Degraded Functionality*** | R=  MTTF= | R=  MTTF= |

{Insert Reliability Graphs and comment them in the text. Make sure that the caption numbers are correct.}

# Discussion

{Discuss the pros and cons of the different design solutions.}

# Conclusions

{Present your conclusions and recommendations.}

**References**

{Use the Vancouver/IEEE style for referencing. For more information please check: <http://www.lib.unimelb.edu.au/cite/ieee/index.html>

For an example of how to write references, see Kopetz and Bauer [1]. (This paper is part of the course literature and is published by the Institute of Electrical and Electronics Engineers, Inc, known as IEEE, and therefore follows the IEEE format for scientific journal papers. Other publishers use slightly different formats.)

[1] H. Kopetz and G Bauer, “The Time-Triggered Architecture,” Proceedings IEEE, vol. 91, no.1, pp.112-126, Jan 2003}