IT-universitetet i Göteborg

CHALMERS | GÖTEBORGS UNIVERSITET

Dept. of Computer Science and Engineering

Course Plan
DIT780

DIT780, Hardware Description and Verification, 7.5 ECTS Credits

Advanced Level

1. Establishment

The Faculty Board at the IT-university established the course plan at 2006-11-17. This course plan is effective from autumn 2007.

Educational area: Technology/Sciences

2. Location

The course is a part of the Computer Science Master´s programme and an elective course at Göteborg University.

3. Knowledge Requirements

The requirement for the course is to have successfully completed an education with a bachelor degree within Computer Science or equivalent. The course requires a basic knowledge of digital design (logic gates, latches, how they are used to build circuits with or without state, the idea of a finite state machine). Familiarity with programming in a functional language is desirable, but not essential. Students with a strong background in digital electronics and the hardware description language VHDL will be able to learn sufficient functional programming in this course, even if they have not seen functional programming before. Other students are advised to take an introductory course in functional programming before taking this course. Similarly, a strong background in functional programming can compensate for a weaker background in digital design. A previous course in logic (DIT201) or in program verification (DIT081) is desirable, but not essential.

4. Learning Outcomes

The aim of the course is to give a flavour of some industrially applied methods for description and verification of hardware, as well as some of the current research in the area. You will be exposed to two different hardware description languages, and to associated verification methods, both in theory and in practice.

After completing the course, you should be able to:

- design and simulate simple circuits in the standard hardware description language VHDL using Gaisler's two process method
- write formal properties of those circuits in the standard property specification language PSL, and verify or disprove those properties using a commercial verification tool
- be able to present and apply the underlying theory and algorithms (the use of binary decision diagrams, state transition systems, CTL model checking, the semantics of PSL)
- design simple circuits by using the Lava system to write circuit generators

- use both simulation and formal verification to verify properties of those circuits in Lava
- be able to briefly describe the underlying verification method (SAT-based induction)
- concisely explain the advantages and limitations of each of the above two design flows
- be able to place the above methods in the context of current industrial practice in hardware verification

5. Content

We typically have lectures not only from Chalmers staff but also from experts working in industry on hardware design and verification.

6. Literature

See separate literature list.

7. Examination

The examination consists of 3 parts: two Labs, two Take-Home Exams, and one written exam. The take home exams will each contribute 25% to your final grade, but you must also pass both of them. The written exam will contribute the remaining 50%. You must also pass the labs. Labs may be done in pairs, but Take-Home Exams must be done alone.

8. Marks

The course is graded with the following marks: Fail, Pass, Pass with Distinction. The course can also, at the students' request, be marked according to ECTS standards.

9. Evaluation

The course is evaluated through meetings both during and after the course between teachers and student representatives. Further, an anonymous questionnaire can be used to ensure written information. The outcome of the evaluations serves to improve the course by indicating which parts could be added, improved, changed or removed.

10. Other

The course is held in English.