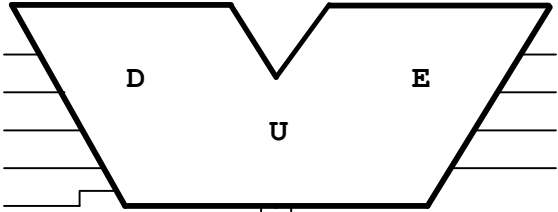


function				operation
f_3	f_2	f_1	f_0	<i>RTN</i>
0	0	0	0	$U=0$
0	0	0	1	$U=FD_{16}$
0	0	1	0	$U=FE_{16}$
0	0	1	1	$U=FF_{16}$
0	1	0	0	$U=E$
0	1	0	1	$U=D_{1k} + C_{in}$
0	1	1	0	$U=D \vee E$
0	1	1	1	$U=D \wedge E$
1	0	0	0	$U=D \oplus E$
1	0	0	1	$U=D + C_{in}$
1	0	1	0	$U=D + FF_{16}$
1	0	1	1	$U=D + E + C_{in}$
1	1	0	0	$U=D + E_{1k} + C_{in}$
1	1	0	1	$U=D \ll 1 (C_{in})$
1	1	1	0	$U=(C_{in}) D \gg 1$
1	1	1	1	$U=(d_7) D \gg 1$

Arithmetic Logic Unit



ALU control



Common clock

Memory

