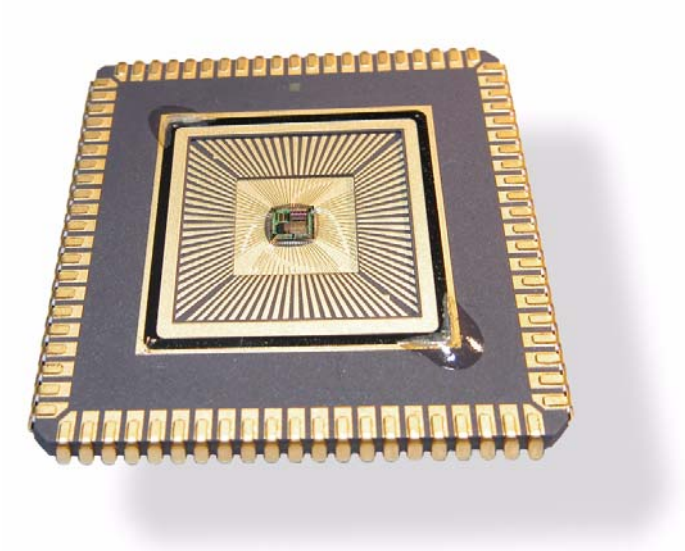
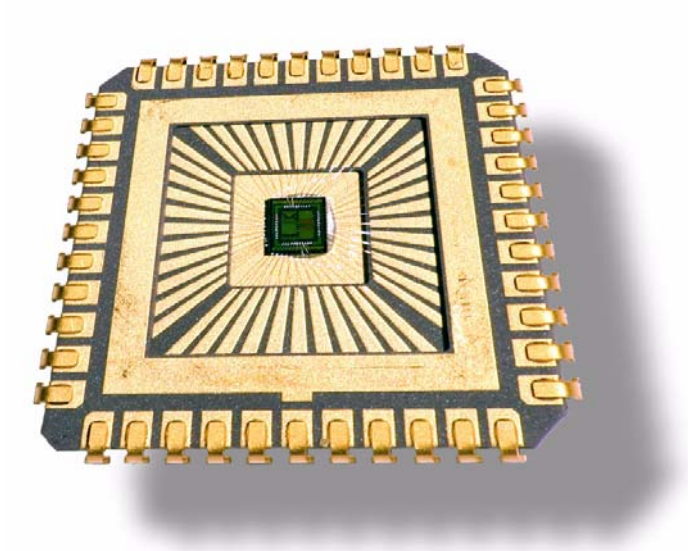
Design of ASICs





Professor Per Larsson-Edefors
VLSI Research Group / Integrerade elektroniksystem

OUTLINE

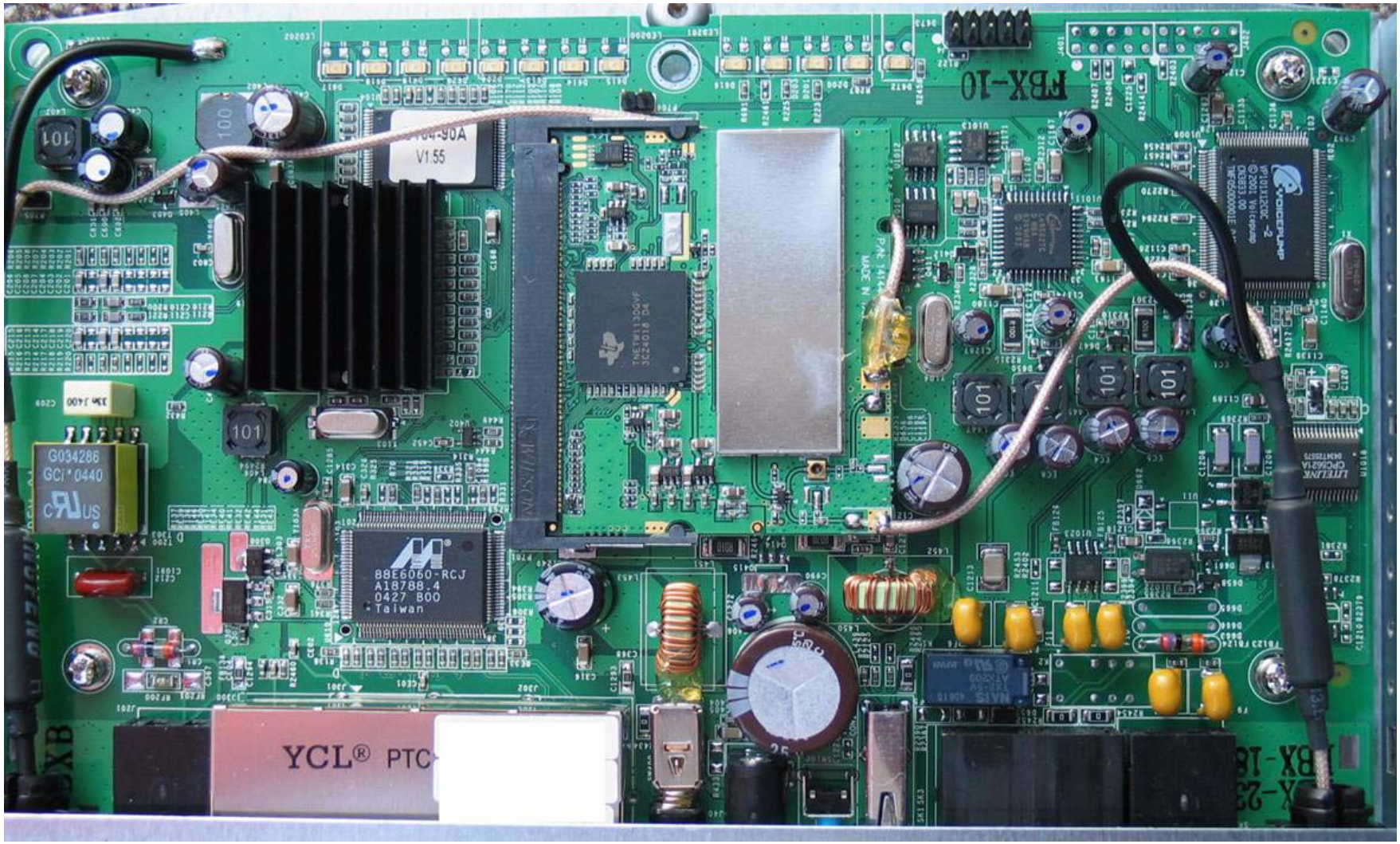
- Introduction.
- IC categories, CMOS and its electrical features.
- Evolution of ASICs.
- Adder case study.

Learn more - Integrated Electronic System Design (IESD)

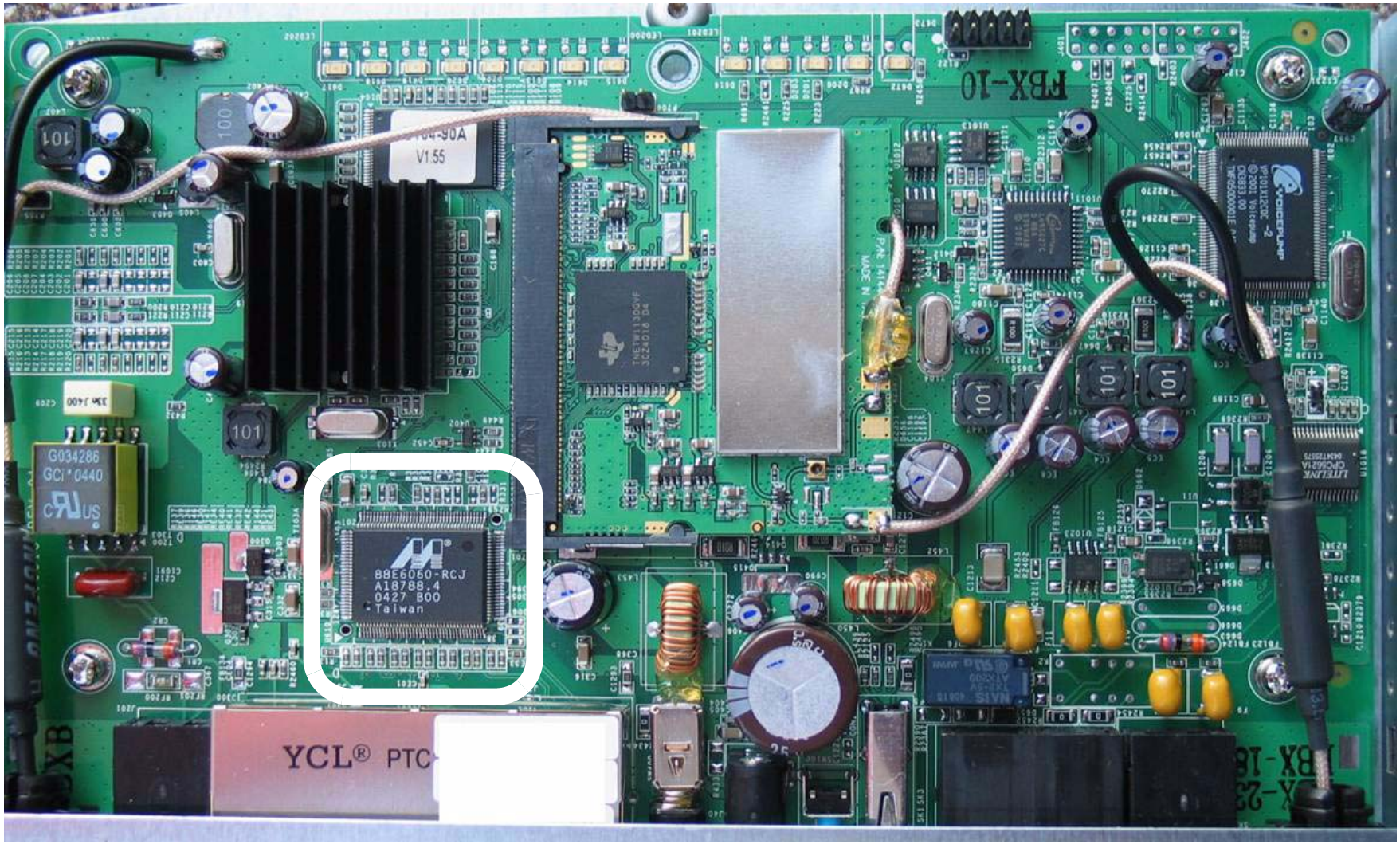
Introduction

A Common Application - A WLAN DSL Unit

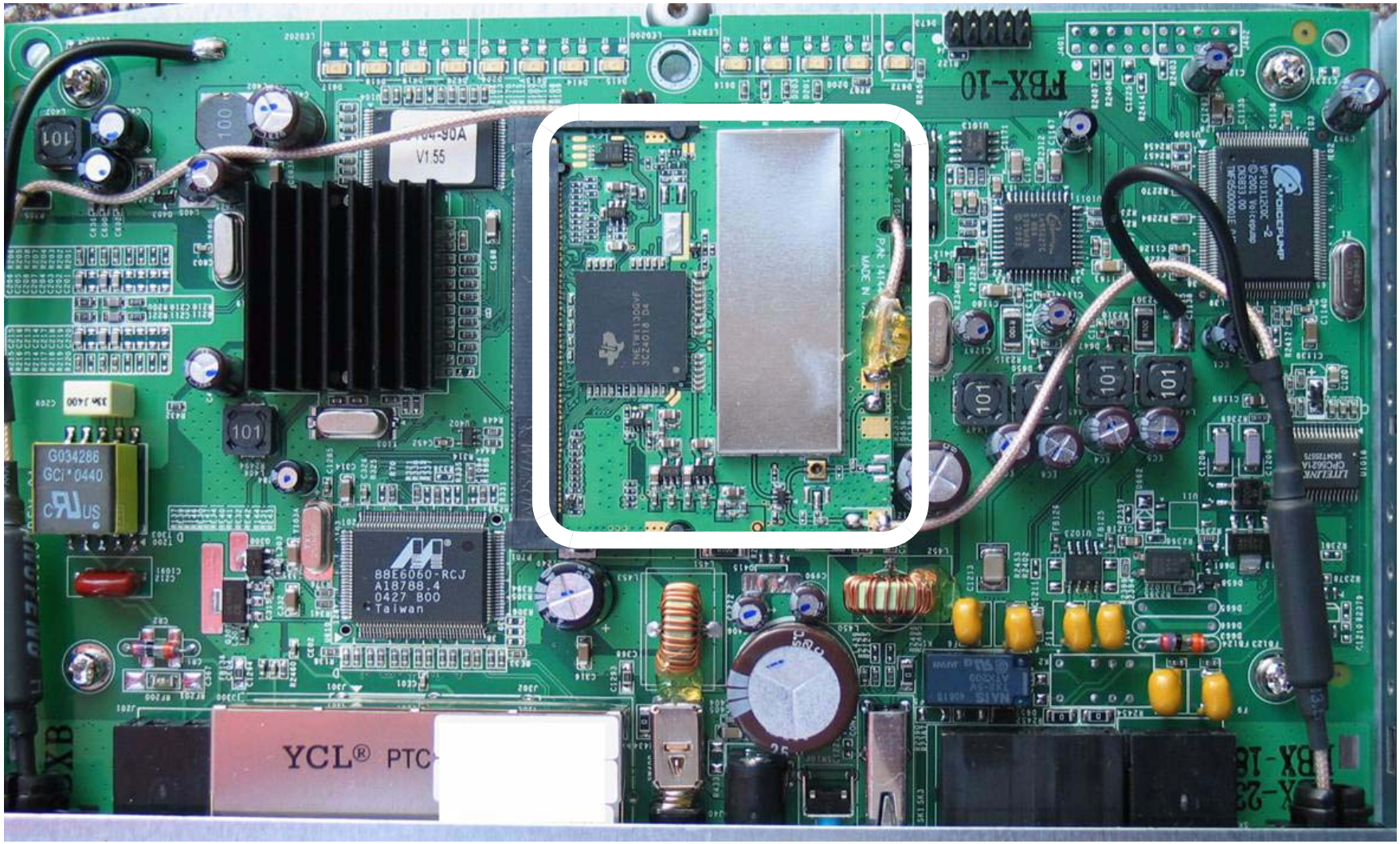
Open up the Unit ... the Front of the Board



… Ethernet Switch from Marvell



… WLAN MAC/Baseband Processor from TI



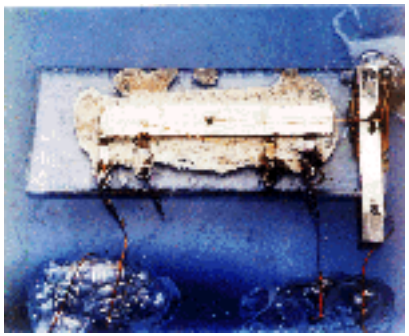
A Digital System

- Racks, card cases, ...
- Power supplies.
- Connectors and cables.
- Printed circuit boards.

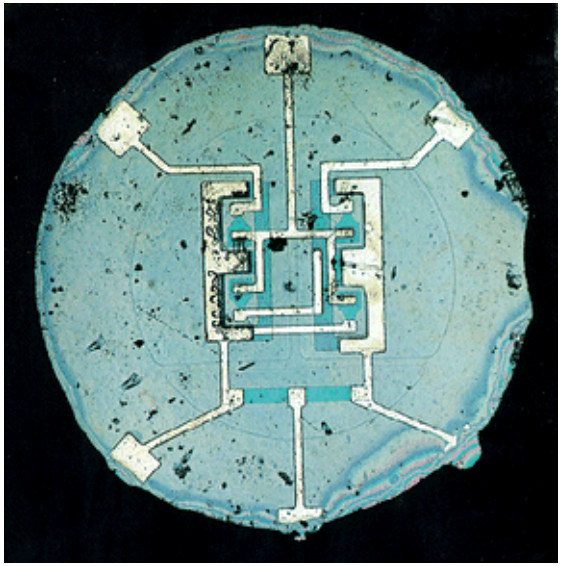
and (loads of)

- Integrated circuits (ICs).

The Early ICs



Jack Kilby's IC (oscillator)
(1958)



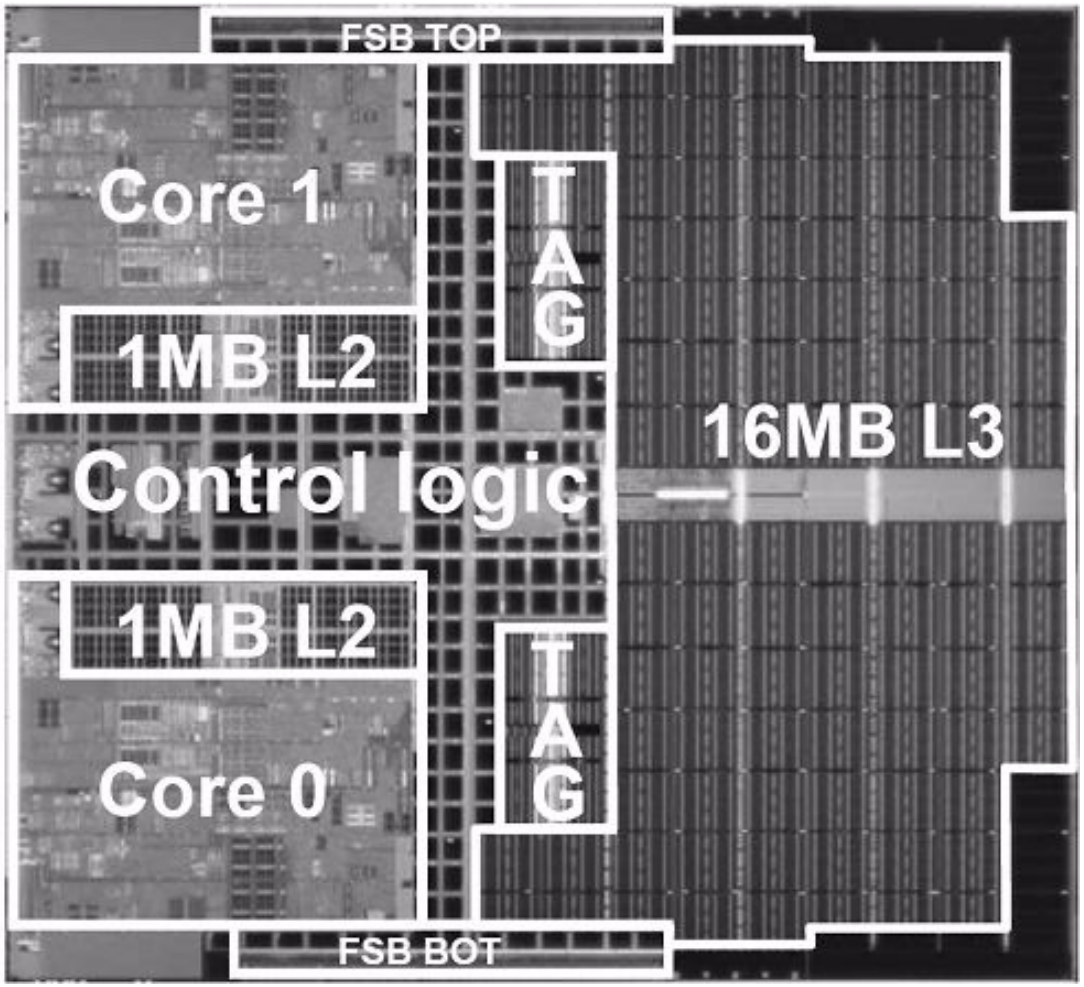
Fairchild IC: RTL logic
(1961)

PENTIUM 4

- 42 million transistors.
- L = 0.18μm.
- 2000.

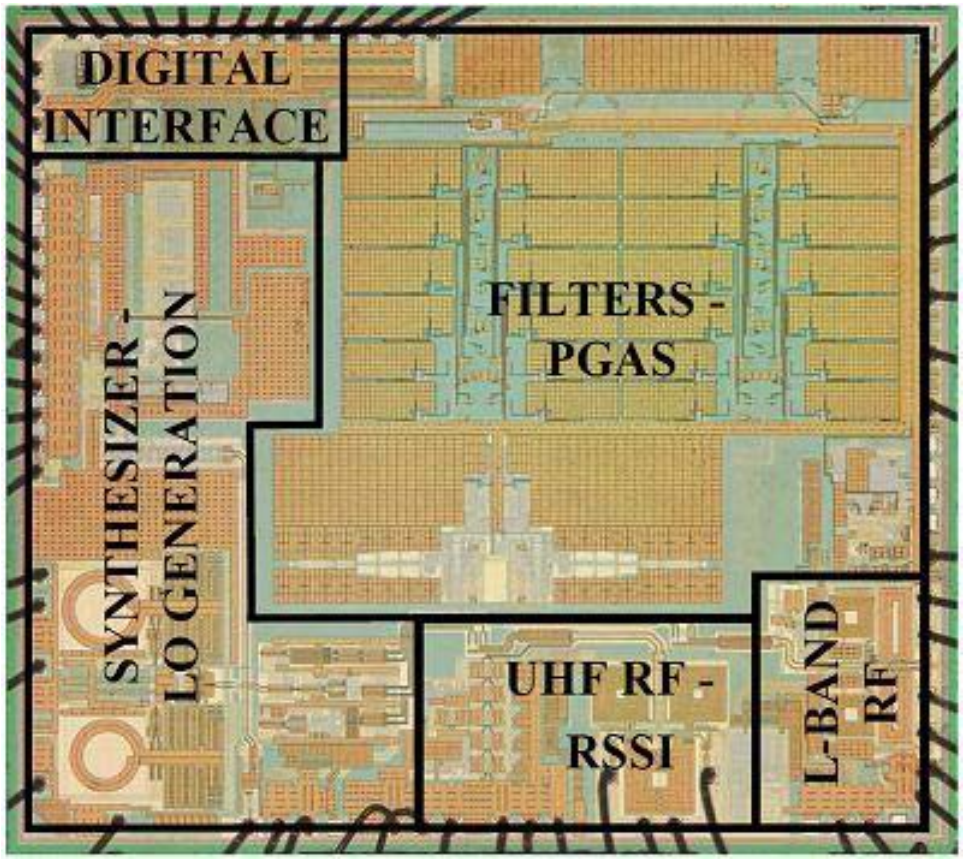
source: Intel

65-nm Dual-Core Xeon (Tulsa) w/ 12MB Cache



source: Intel 2006/2007

A Complete DVB Tuner on One Single ASIC



source: ISSCC06

IC Categories, CMOS and its Electrical Features

Customers' View of Electronics

1. Low cost - customers won't accept excessive prices.
2. Functionality - customers like to have many functions.
3. Flexibility - customers like to have ever changing products.
4. Performance - customers like to have exciting functions.
5. Size and power - customers like to have portable electronics.
6. Reliability - customers like to have working electronics.

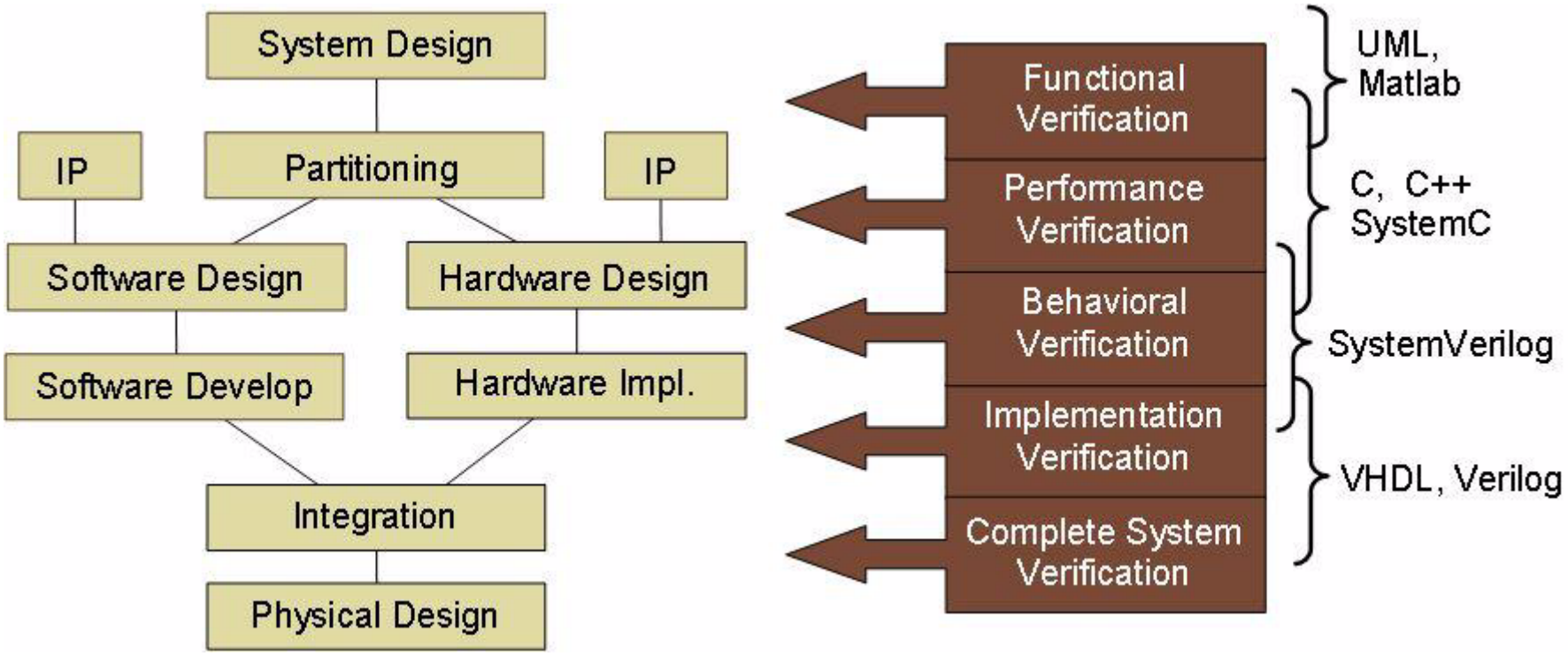
The commodity market today rules our area of engineering

Designers' View of Electronics

1. Low cost - we need to **work fast** and **buy cheap infrastructure.**
2. Functionality - we need to have **large systems.**
3. Flexibility - we need to work creatively with **hardware and software.**
4. Performance - we need to obtain **high speed.**
5. Size and power - we need to target **low power.**
6. Reliability - we need to make **no mistakes.**

1 + 2 + 3 + 4 + 5 + 6 = Challenging electronics design

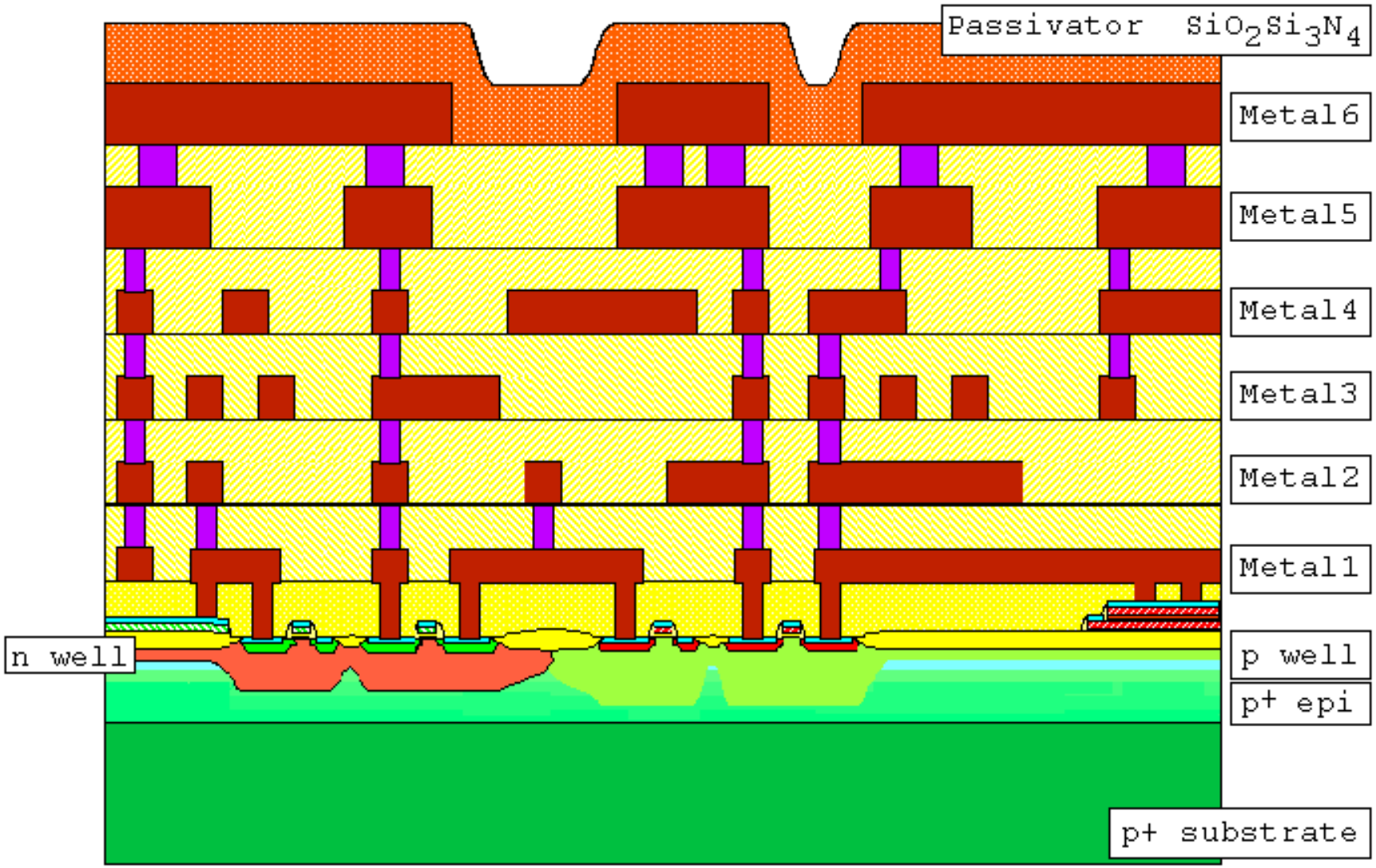
MANY DESIGN LEVELS/MANY TOOLS - SW TO HW



What IC Technology Should You Use ?

- Application specific ICs (ASICs).
  - custom designed, synthesized or a mix.
- Application Specific Standard Products (ASSPs).
  - often standard microprocessors (uP) or digital signal processors (DSPs).
- Field programmable logic devices (FPGAs, CPLDs, PALs, PLAs).
  - the hardware structure can be changed by programming interconnects.
- Memory chips.
- Standard low-density components.

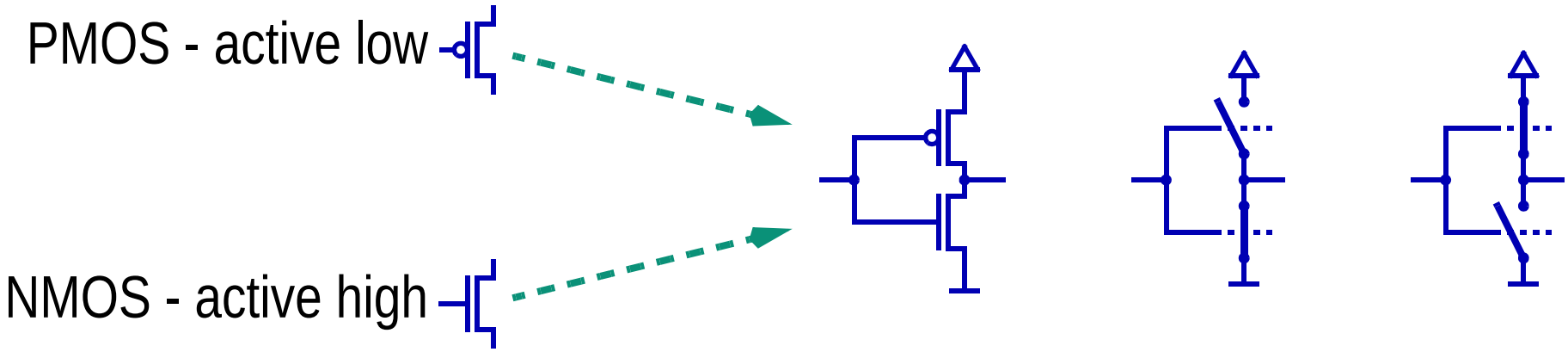
Example of CMOS Process (Cross Section)



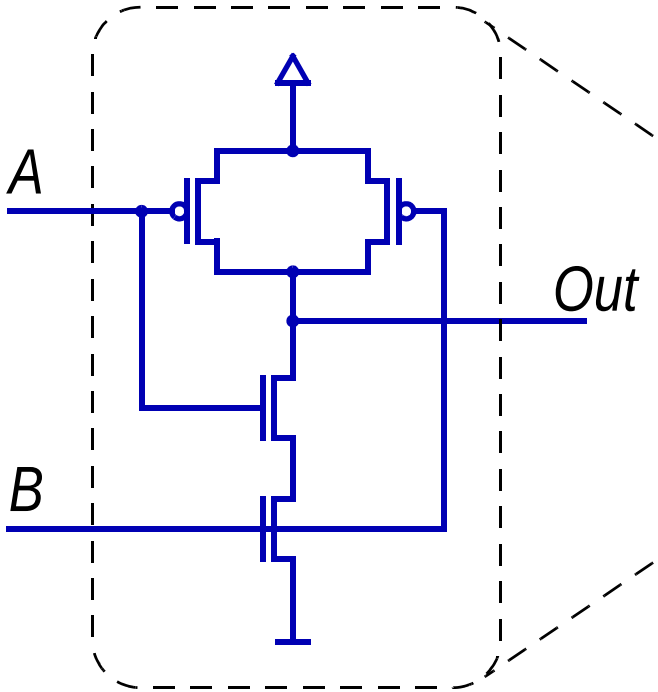
The Concept of CMOS (1963)

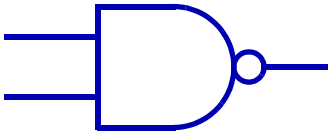
Metal-Oxide-Semiconductor
Field Effect Transistor
(MOSFET)

Complementary MOS
=
CMOS



A 2-input CMOS NAND Gate

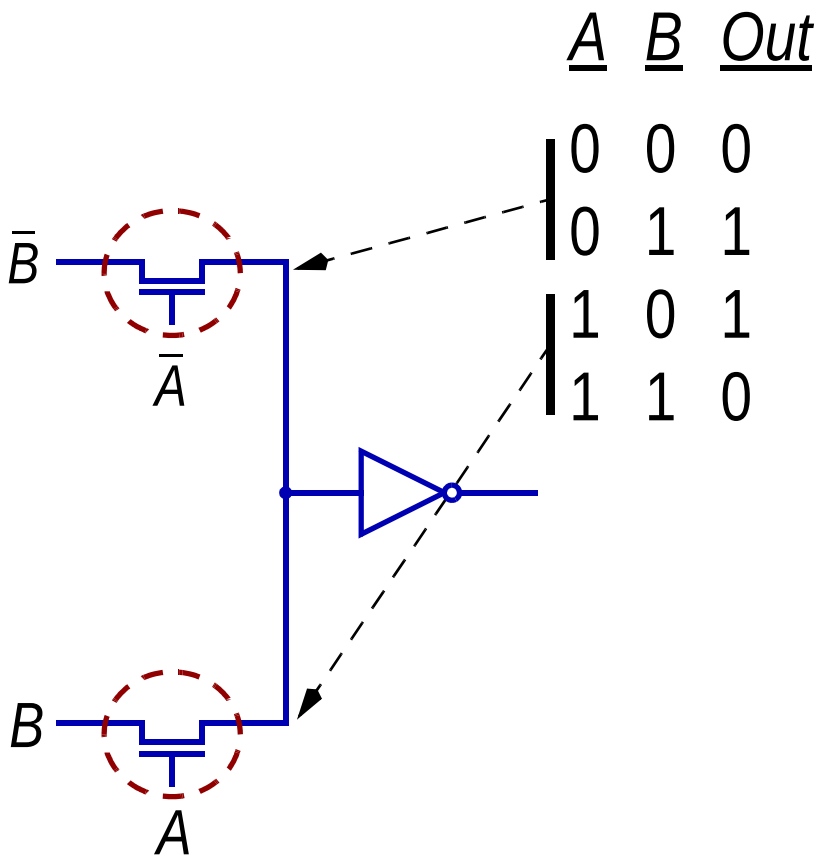




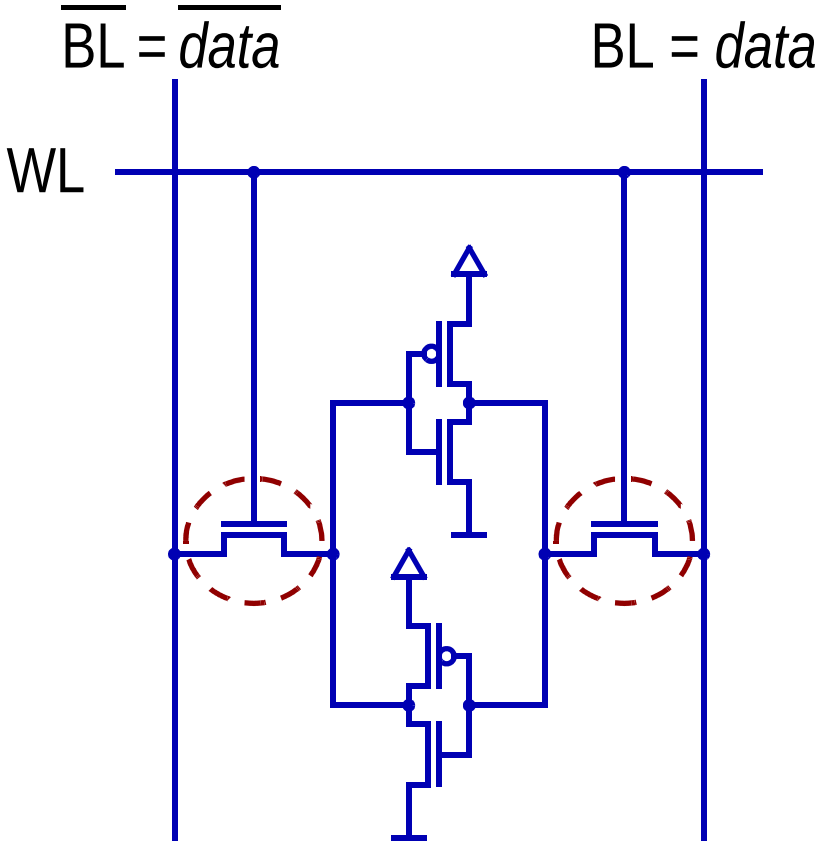
A	B	Out	NMOS	PMOS
0	0	1	OFF	ON
0	1	1	OFF	ON
1	0	1	OFF	ON
1	1	0	ON	OFF

Pass Transistors - Alternate CMOS

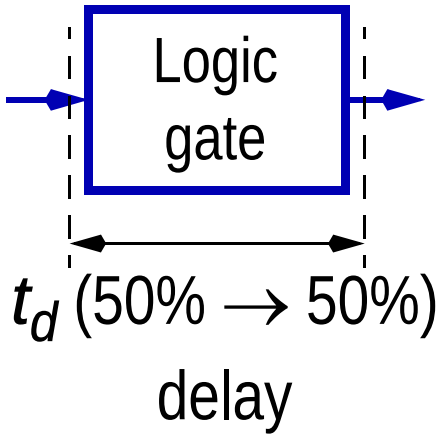
- PTL = Pass Transistor Logic

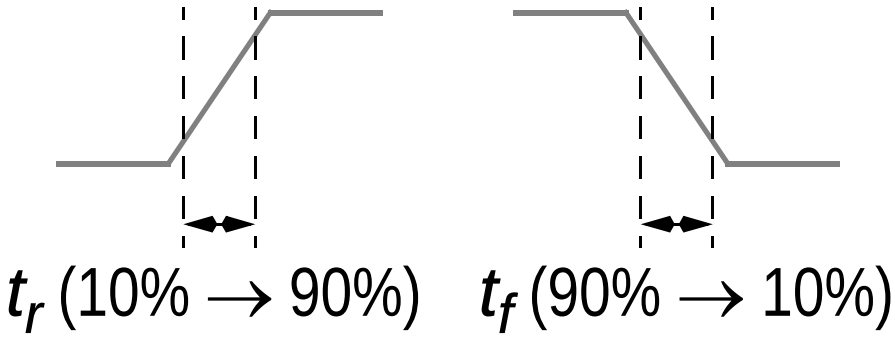


- Pass transistors of SRAM cell

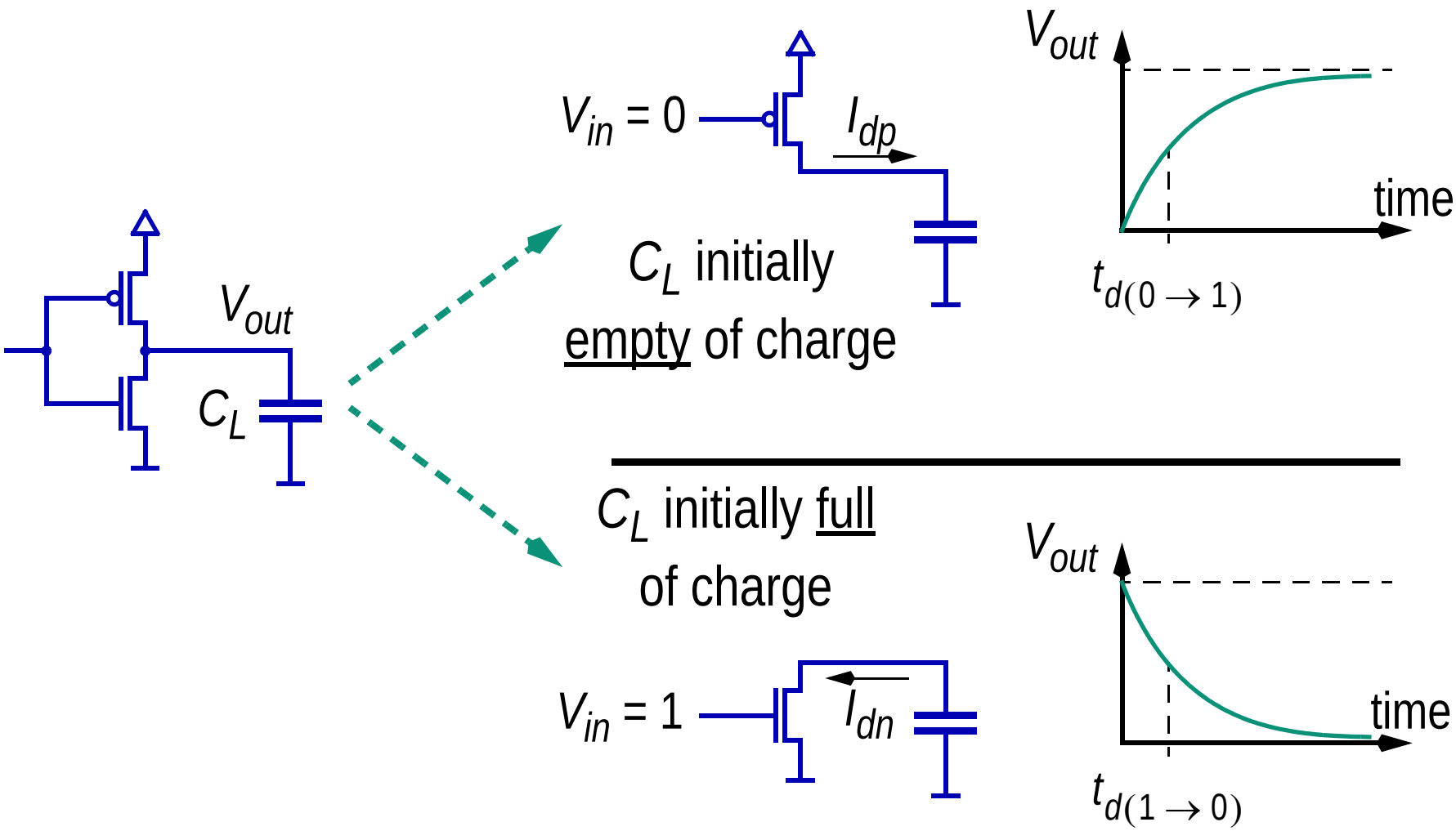


Gate Properties - Delay, Rise- and Fall Time



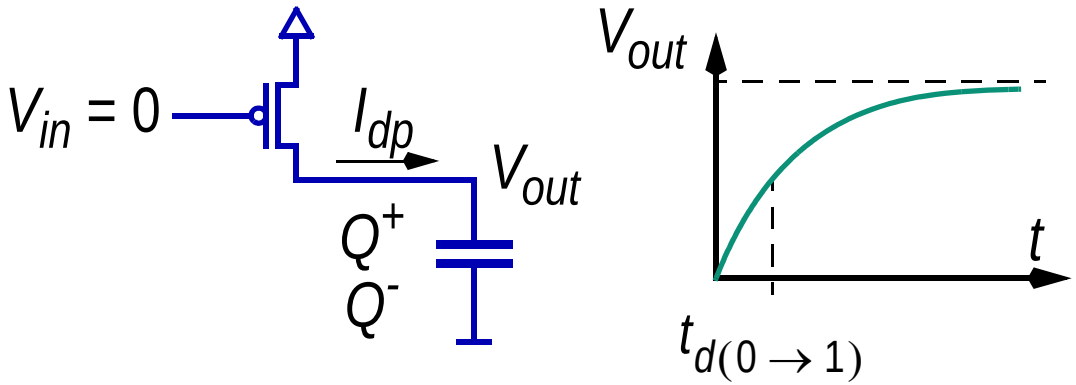


DELAY: CHARGING AND DISCHARGING



First-Order Inverter Delay

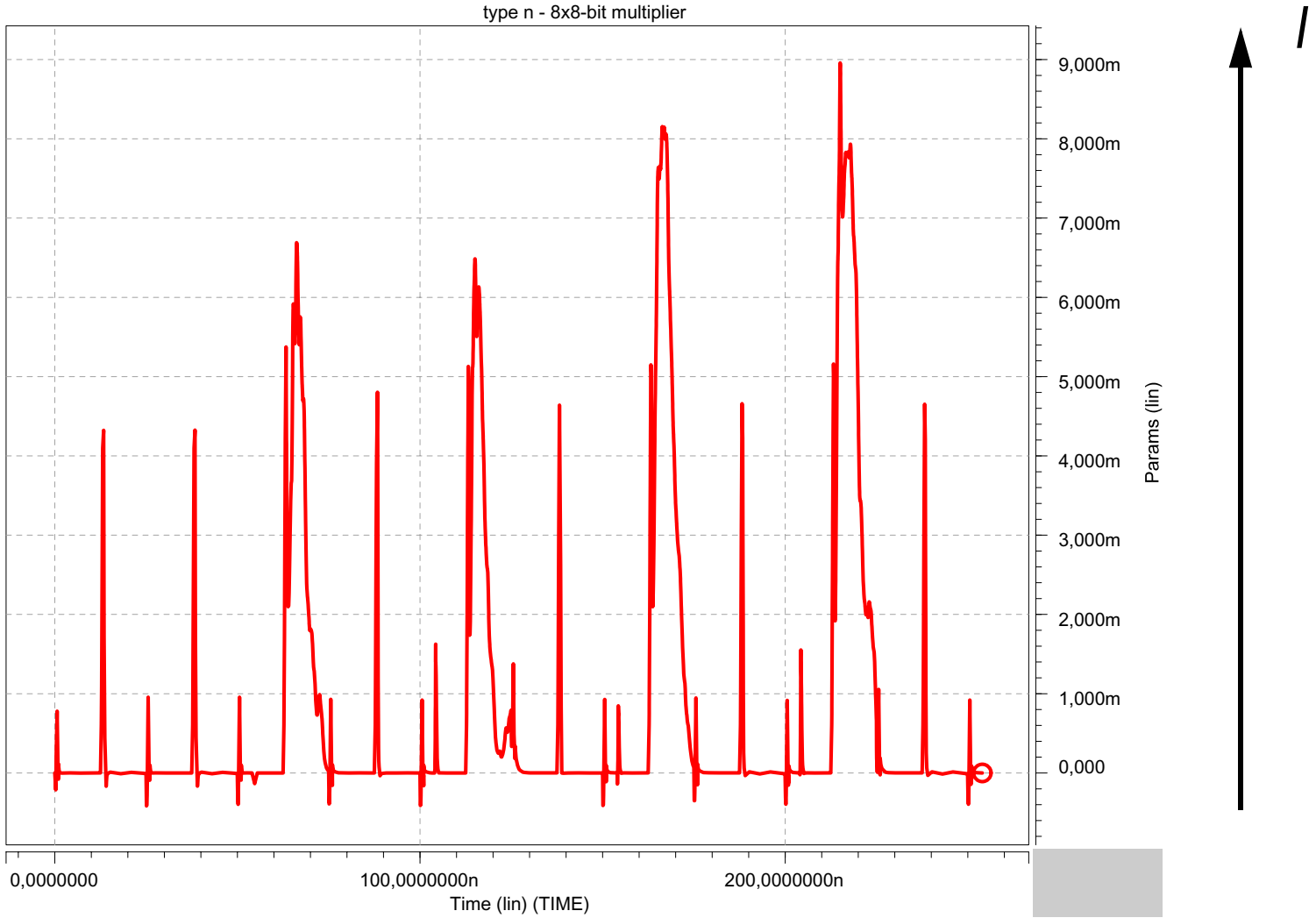
- What is the charging time $t_{d(0 \rightarrow 1)}$ depending on?



- $$t_{d(0 \rightarrow 1)} = \frac{C_L}{k \cdot V_{DD}}$$

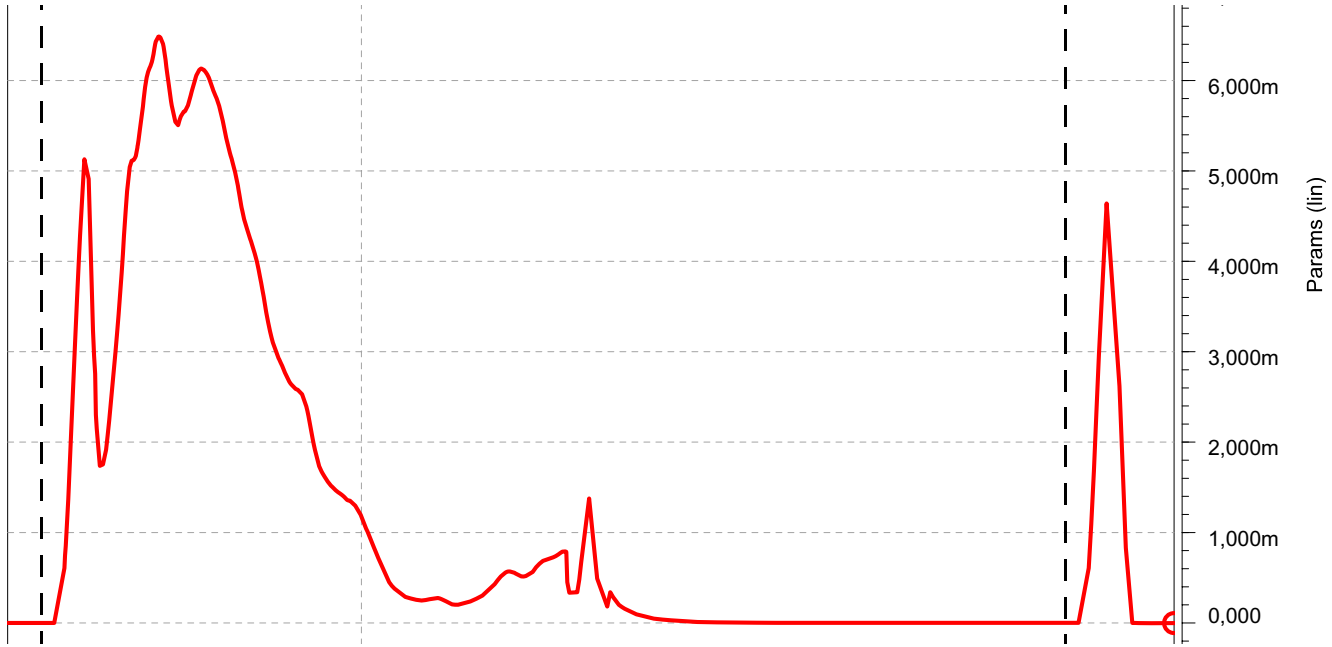
In an ASIC we have excellent control of
C_L and k (through transistor size W) => high speed

Current Drawn during 10 Clock Cycles



Close Up of Current Drawn in One Cycle

- Many gates and a large logic depth leads to current variations from cycle to cycle.
- Average power = average current * supply voltage.

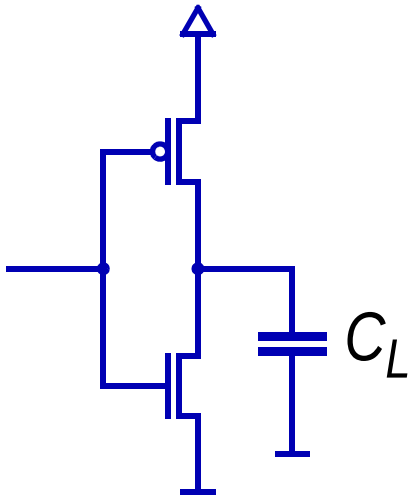


Several Reasons for Power Dissipation

- Dynamic (or active) power.
  - Signal switching (60-80% of total power).
- Static power.
  - Leakage due to subthreshold currents (20-40% of total power).

Leakage power is viewed as one of the major obstacles to further integration

Switching Power



- $E = Q \cdot V_{DD} = (C_L \cdot V_{DD}) \cdot V_{DD}$

  During output signal switching, energy E is converted to heat.

- Energy represents power dissipated for some time duration (e.g. a clock period T):

  $E = T \cdot P_{sw}$ or (using frequency f)

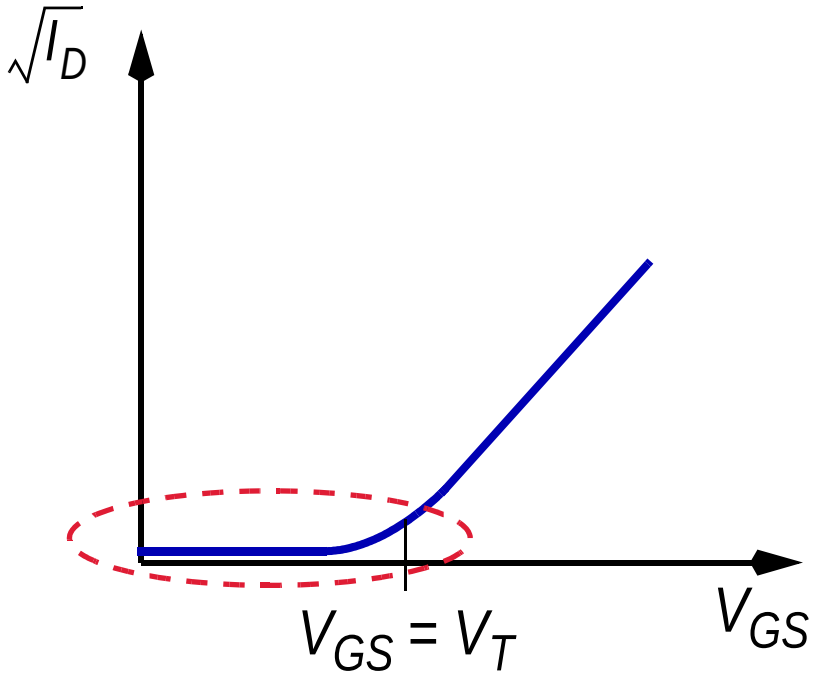
  $$P_{sw} = \frac{1}{T} \cdot V_{DD}^2 \cdot C_L = f \cdot V_{DD}^2 \cdot C_L$$

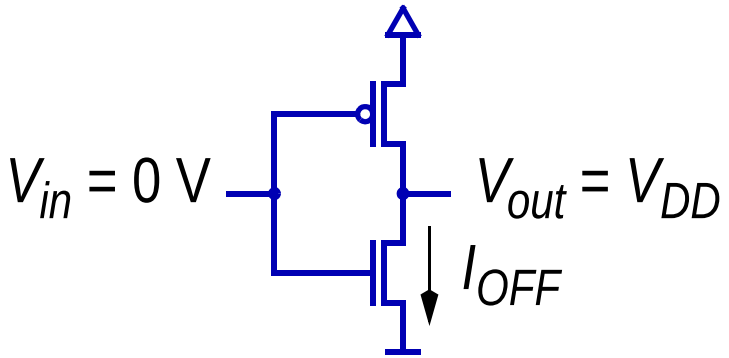
In an ASIC we have excellent control of C_L => low power

Subthreshold Leakage

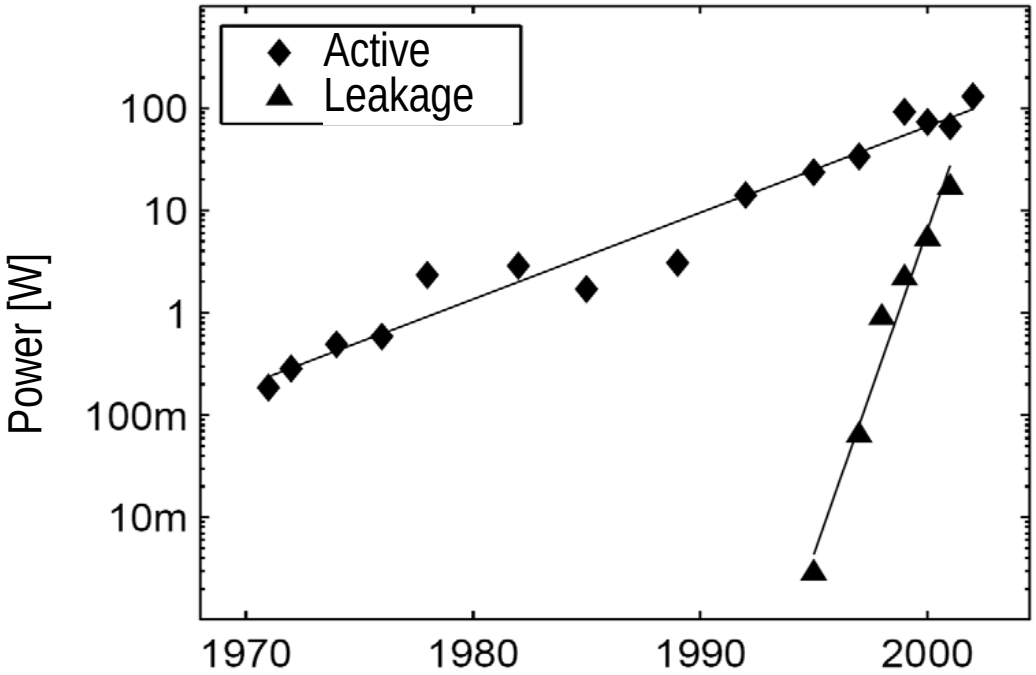
- The subthreshold leakage current depends exponentially on voltage when the transistor voltage is in the region between OFF and ON.

Previously we have viewed transistors as switches,
but now they are dimmers that can never be shut off



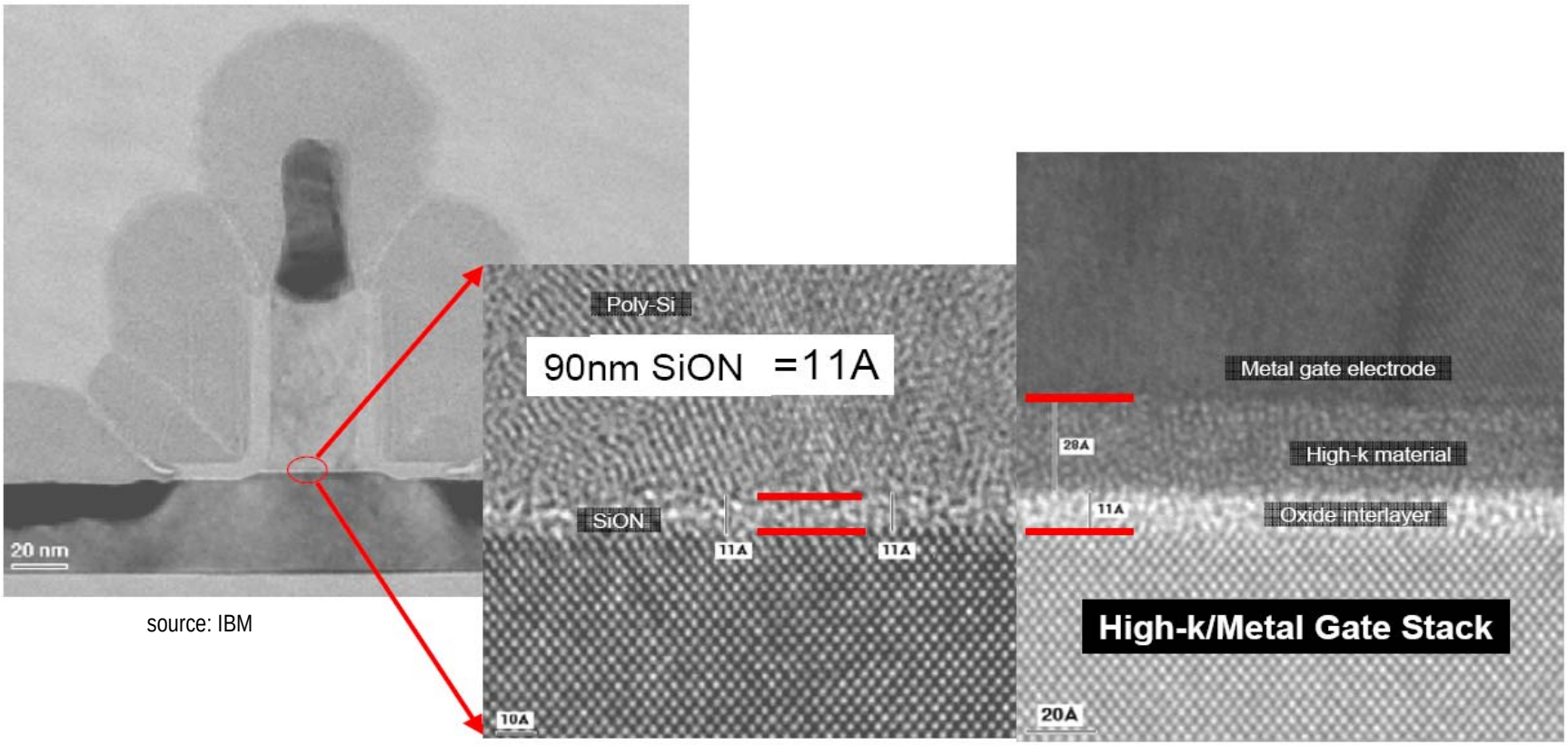


Leakage Trends



Small Devices

- Quantum mechanics - the current tunnels through thin transistor insulator.

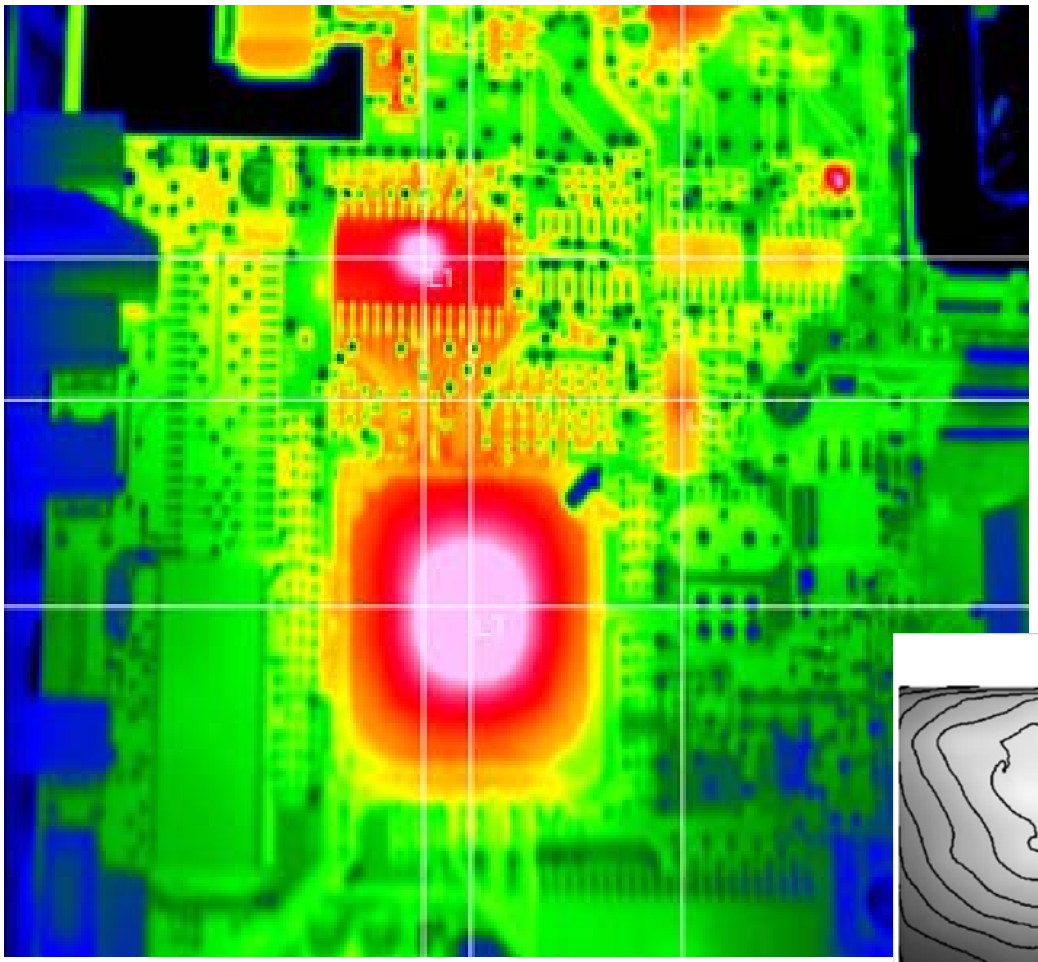


source: IBM

90nm Gate Dielectric:
Tinv = 19A
ToxGL = 11A

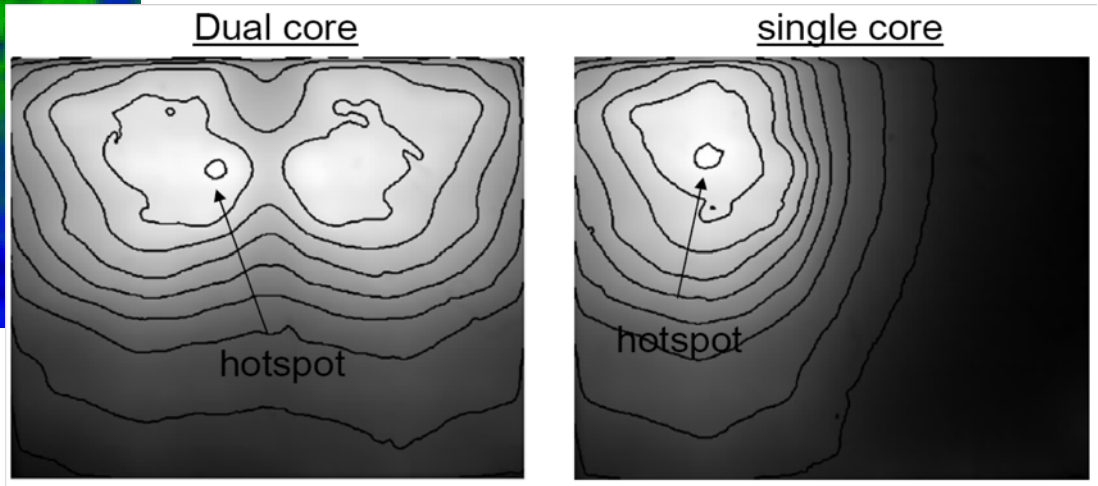
High-k/Metal Gate Stack:
Tinv = 15.5A
ToxGL = 20A

Other Problems - Controlling Temperature!



- Power dissipation leads to hot spots on boards and chips
- In hot areas leakage increases, which makes the chip hotter :-(
- In hot areas, the risk of hardware malfunction increases

source: IBM



Evolution of ASICs

Evolution of Typical Design - 1980-1990

- System's logic =
  Large Scale Integration (LSI) circuits + "Glue logic".
- Tailored ICs (= ASICs) started replacing glue logic.
  - \+ overall system complexity ↓, unit cost ↓, performance ↑
  - \- development cost (fab + tools) ↑, Time-To-Market ↑

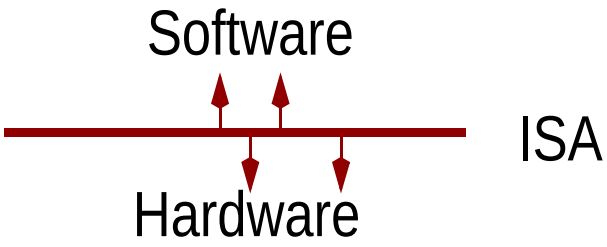
  however, cost was a concern:
  - \- custom-designed IC need large quantities to amortize development cost (= Non-Recurring Engineering).

Evolution, cont. - Meet in the Middle

- Programmable logic!
  - denser than discrete SSI/MSI ICs.
  - programmable logic + CAD-tools + simple “fabrication” => lower NRE and TTM.
  - large volumes requires tailored ICs, because unit cost of programmable logic is high.
  - a number of other issues need to be considered: speed and power dissipation.

Cost vs Performance - Platform Alternatives

ASSP platform	FPGA	ASIC
uP hardware platform + (flexible) software	⟵ compromise ⟶	flexible design method for efficient (fixed) hardware



Hardware specification

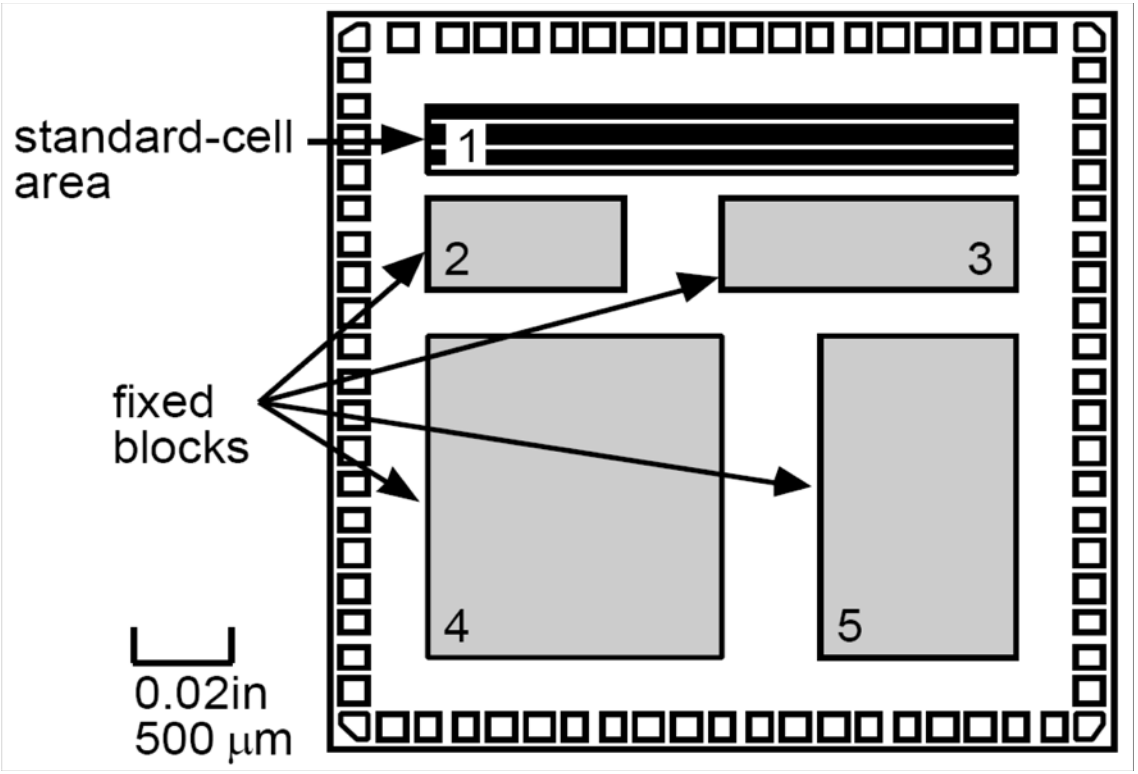
↓

Hardware implementation

Find the appropriate platform while minimizing cost and obeying performance/power constraints

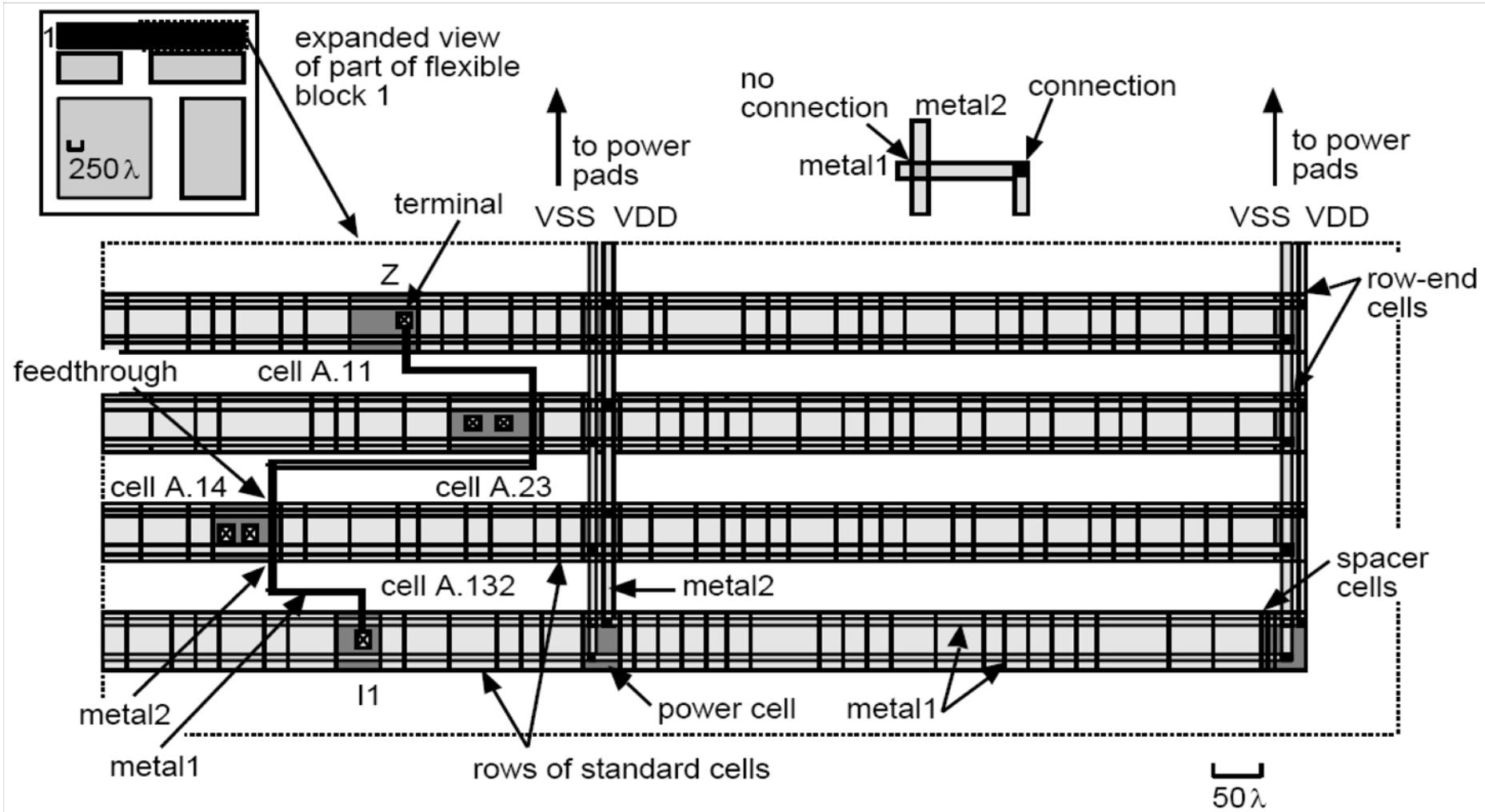
A CELL-BASED ASIC

- A Cell-Based ASIC
  - Library standard cells.
  - Fullcustom blocks, system-level macros, fixed blocks, cores, or functional standard blocks.....
  - All mask layers are customized - transistors and interconnect.
  - Custom blocks can be embedded.

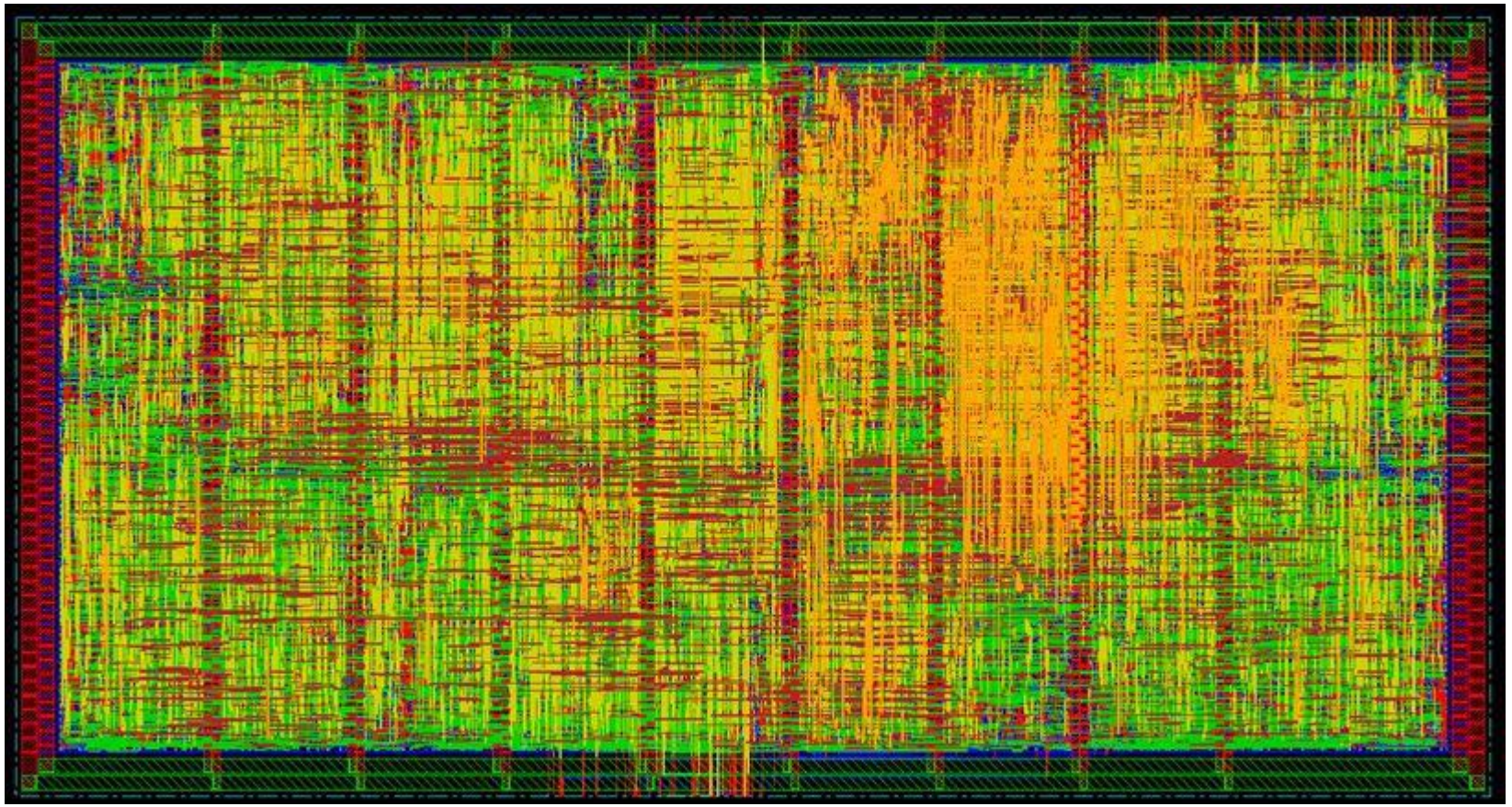


source: M J S Smith

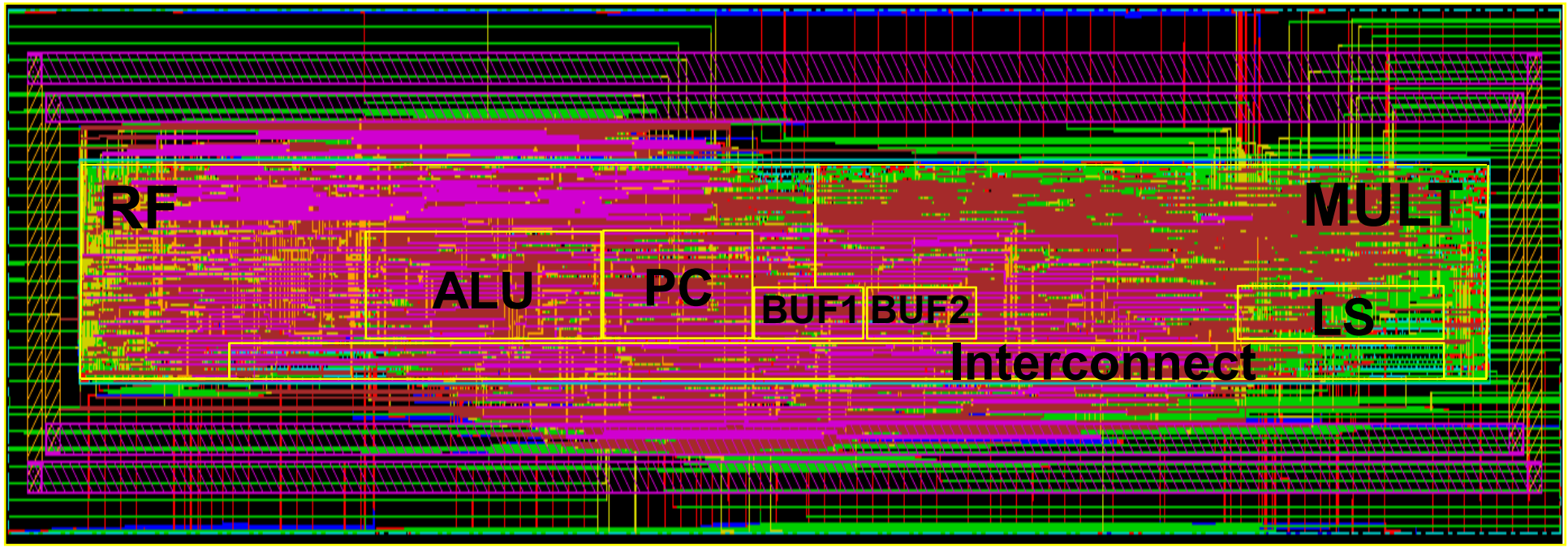
STANDARD-CELL ASIC



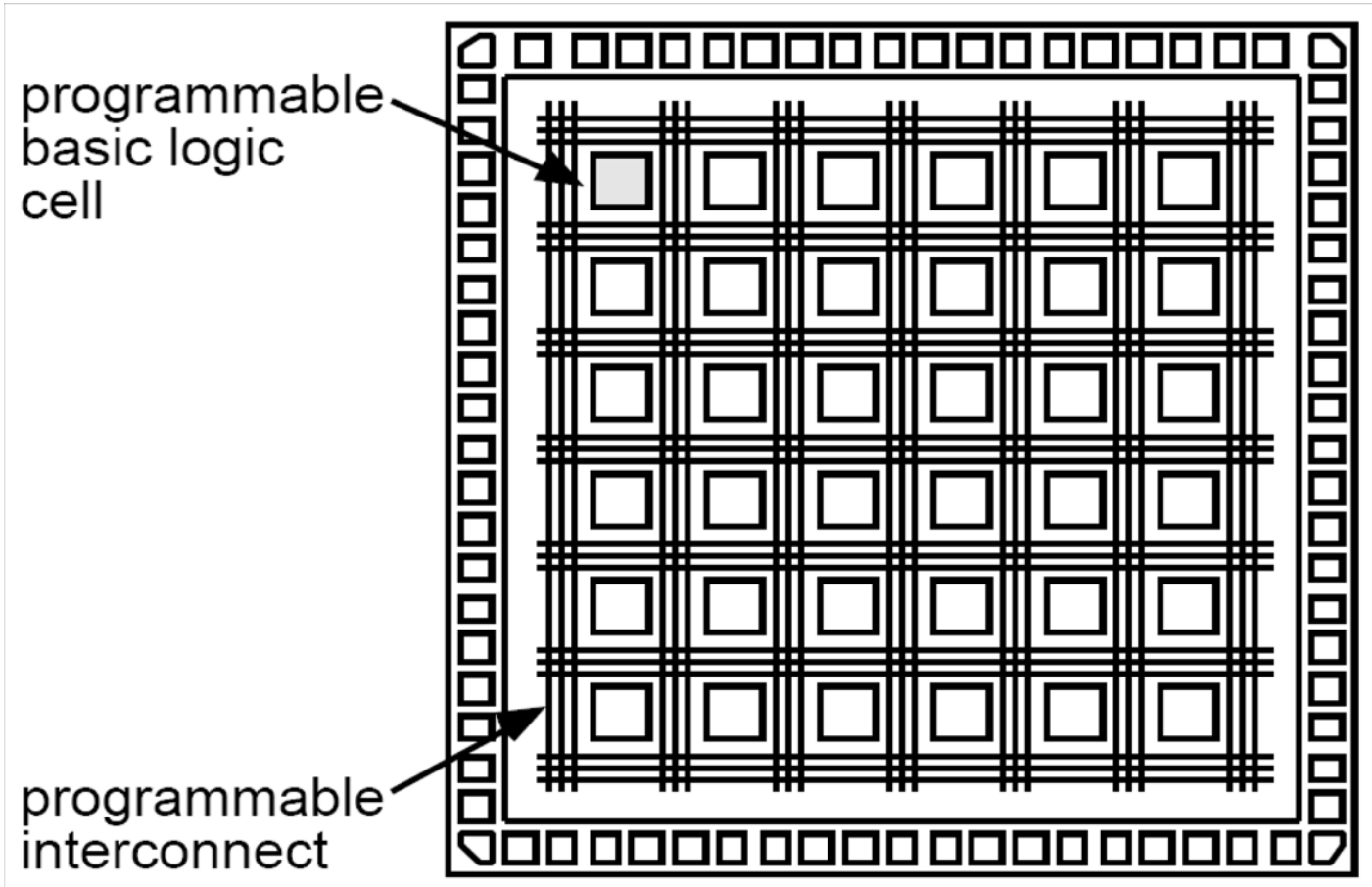
Standard-Cell Design of a Processor



Fresh 65-nm FlexCore Processor



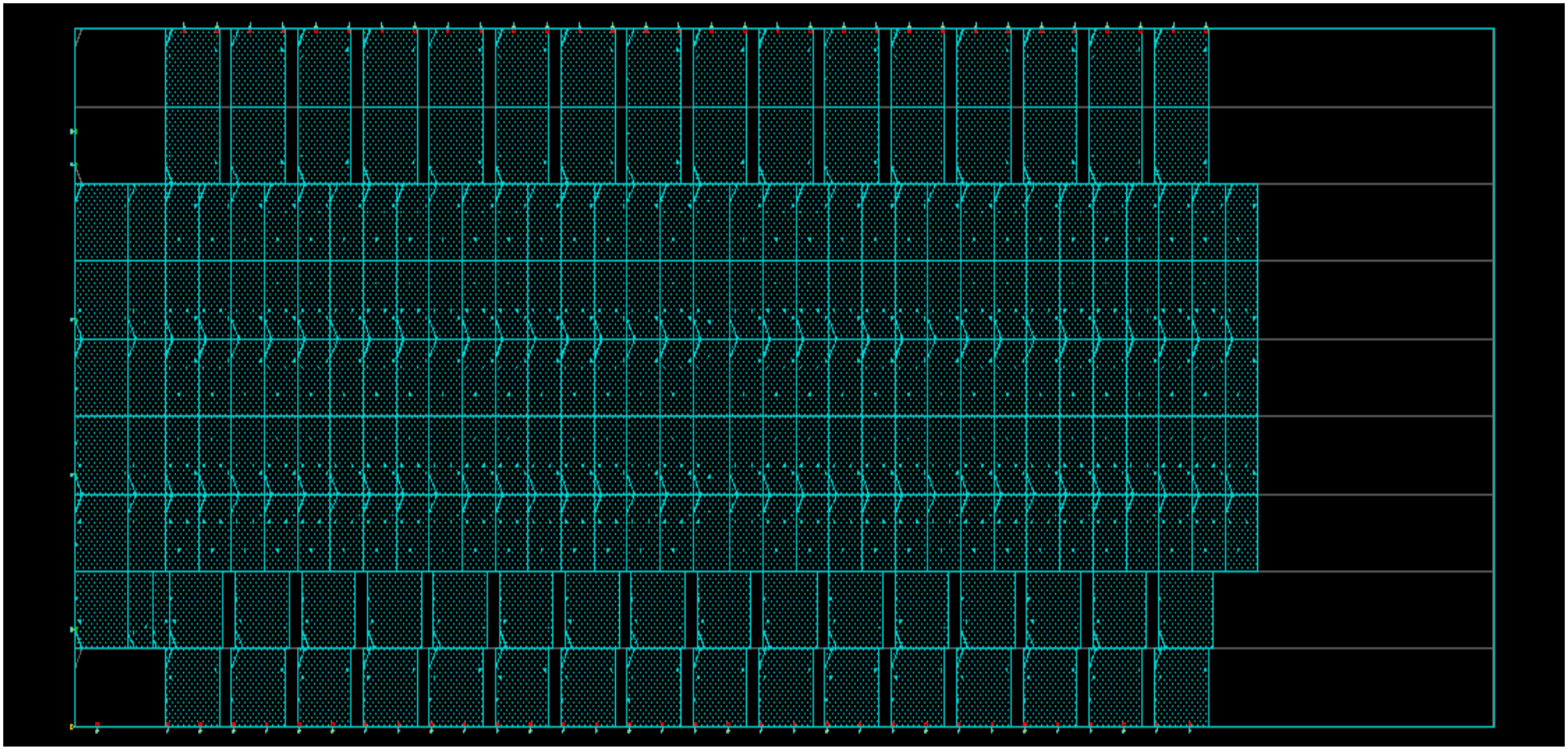
For Comparison ... an FPGA



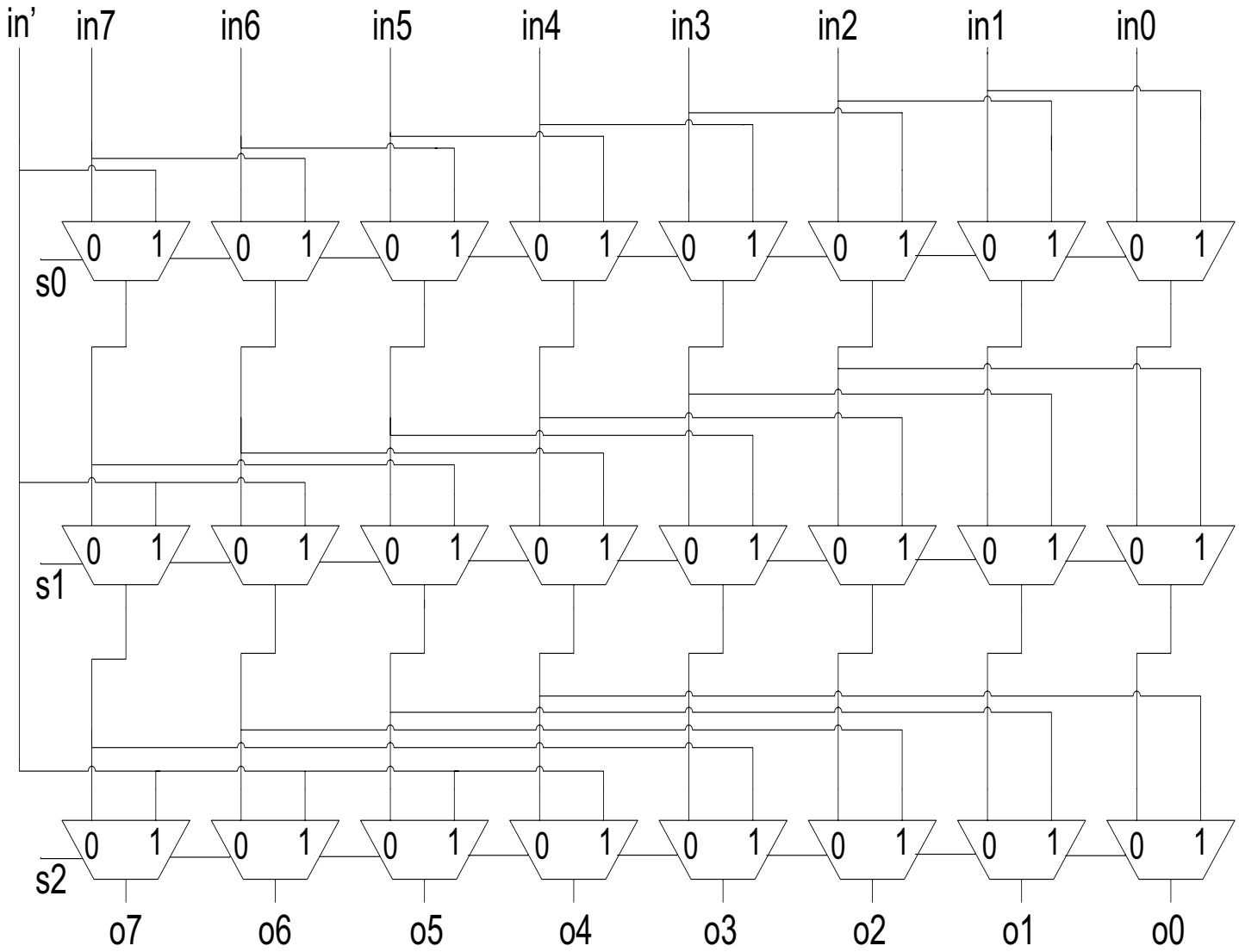
THE FULL-CUSTOM ASIC

- All mask layers are customized in a full-custom ASIC.
- Full-custom offers the highest performance and lowest part cost (smallest die size) with the disadvantages of increased design time, complexity, design expense, and highest risk.
- Microprocessors were exclusively full-custom, but designers are increasingly turning to semicustom ASIC techniques in this area too.

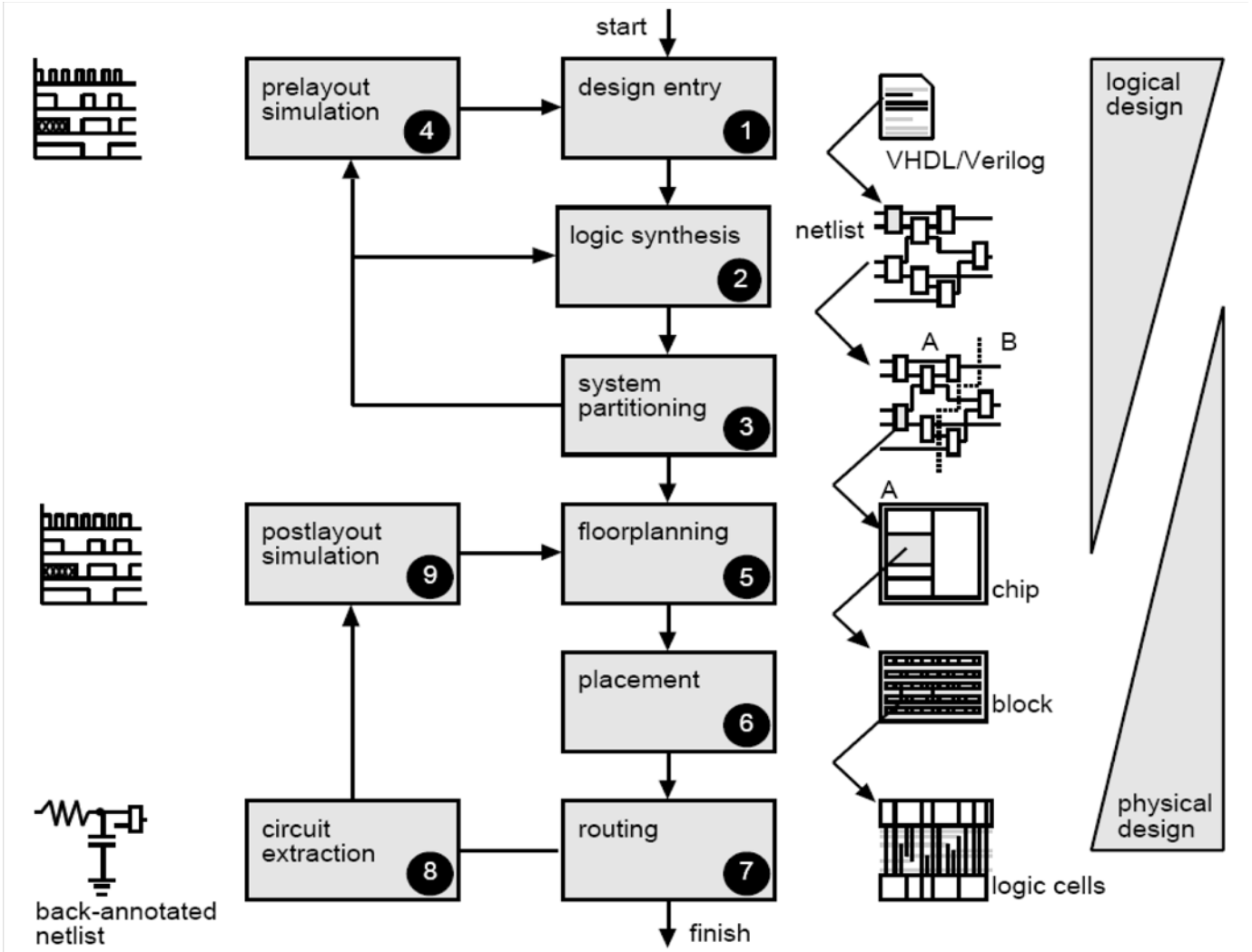
Alternate Layout Schemes



GATE NETLIST LAID OUT

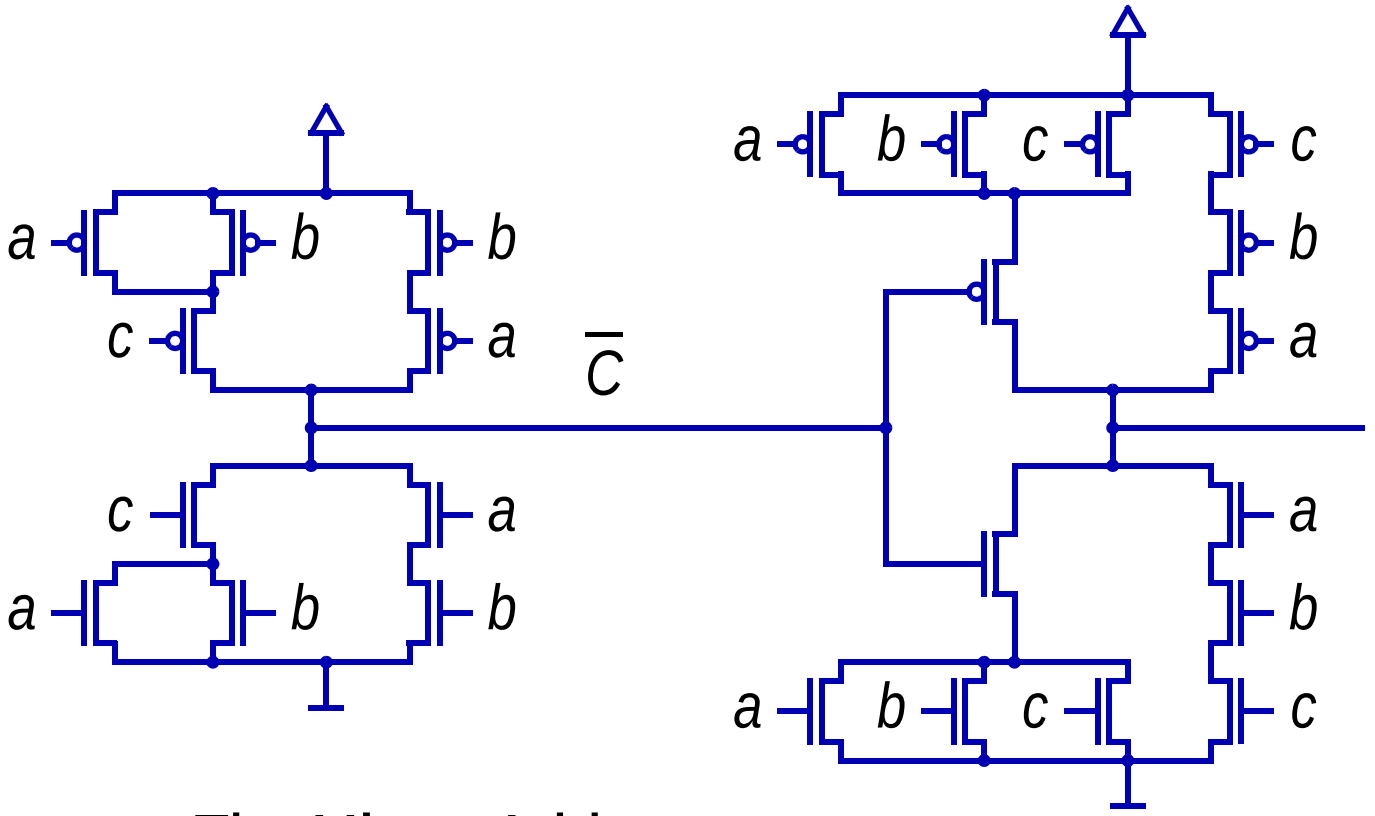


General ASIC Design Flow



Adder Case Study

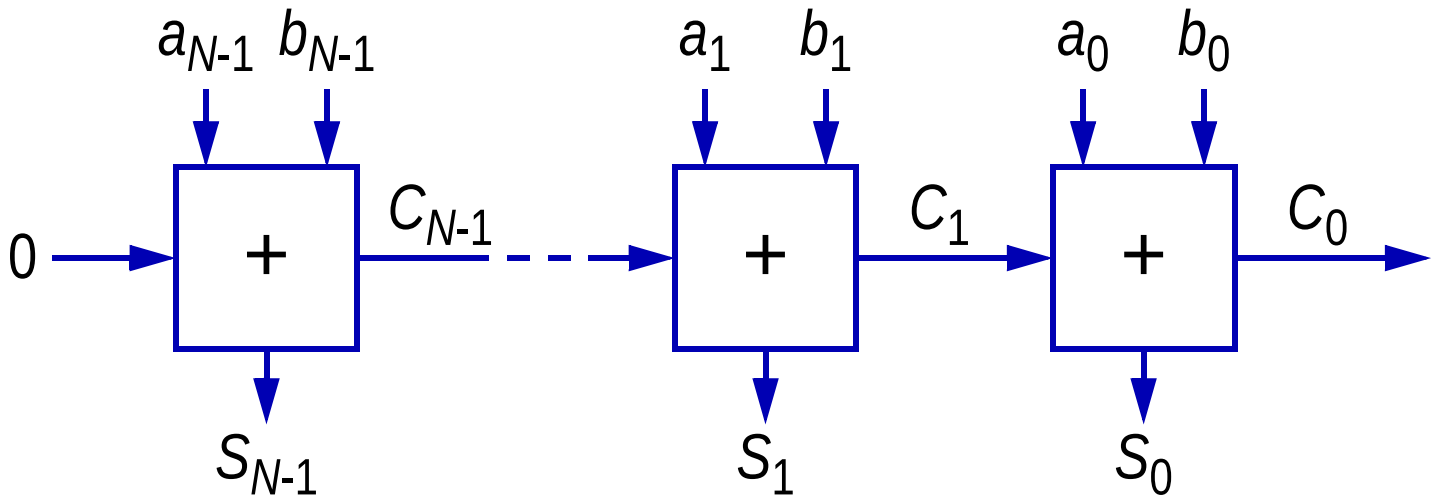
A Full Adder



The Mirror Adder

a	b	c	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

An *N*-Bit Ripple-Carry Adder



Long propagation time due to carry ripple!

$$t_d \propto N$$

Fast Adders Rely on Redefining Adder Signals

Observation:

a and *b* are usually entered in a similar way,
whereas *c* is usually a carry output from a preceding stage.

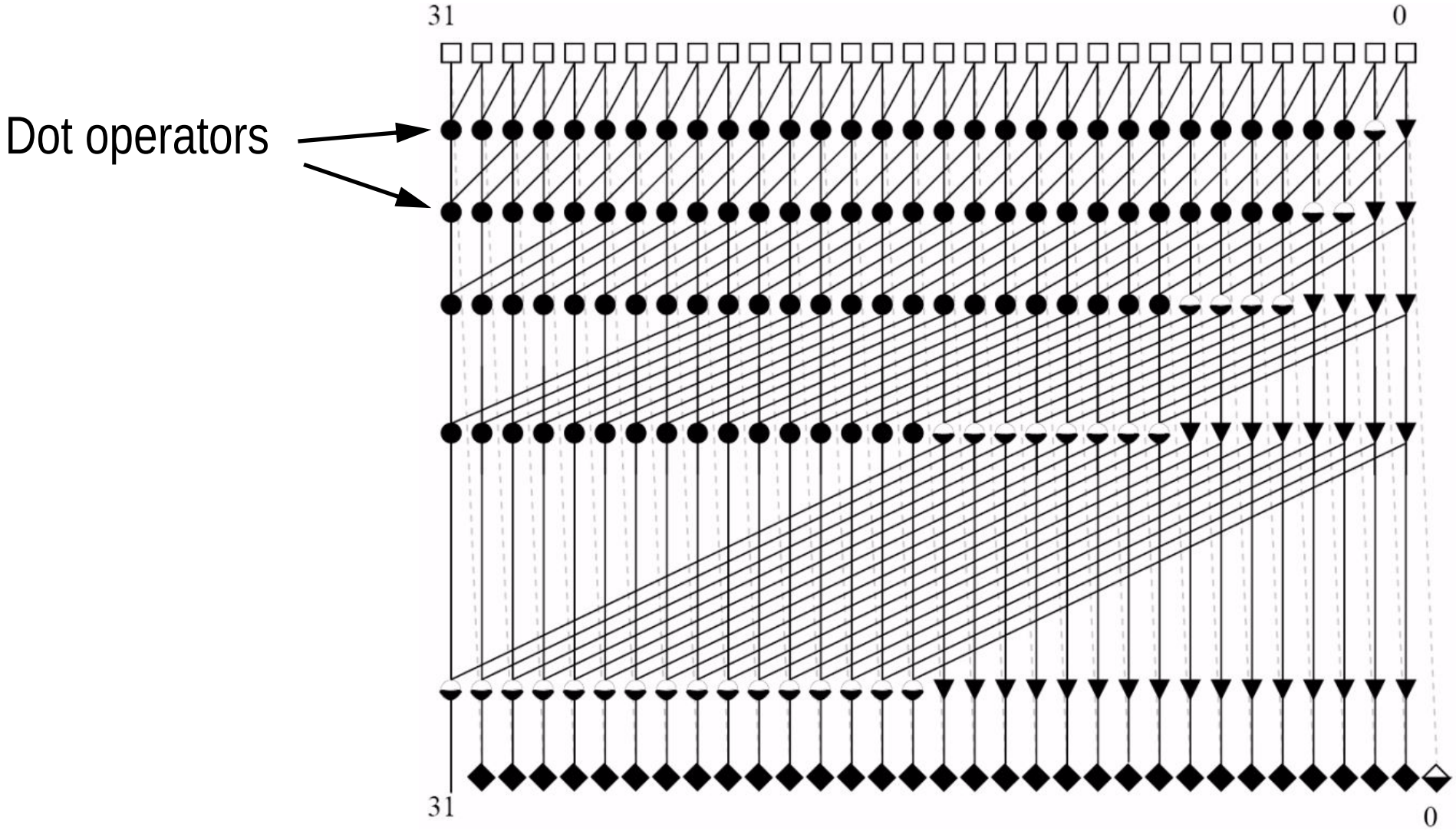
Define two new signals:

- $G = a \cdot b \Rightarrow$ "**Generate** a carry = 1"
- $P = a \oplus b \Rightarrow$ "**Propagate** a preceding carry *c*"

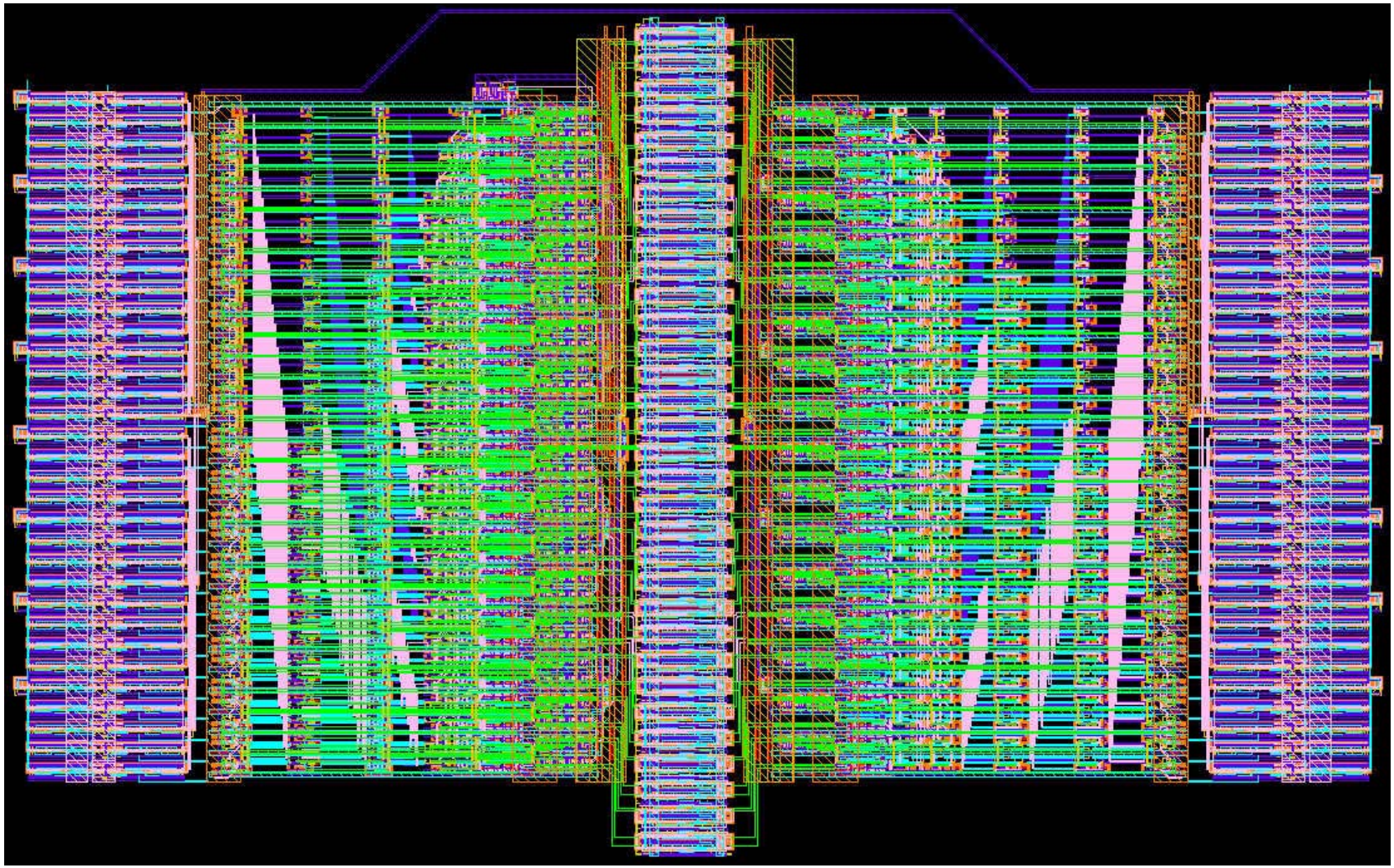
Based on *G* and *P*, we have $S = P \oplus c$ and $C = G + P \cdot c$,
from which lookahead adders are created. For example,

- $C_{IV} = G_{IV} + P_{IV}\,(G_{III} + P_{III}\,(G_{II} + P_{II}\,(G_I + P_I\,C_{in})))$

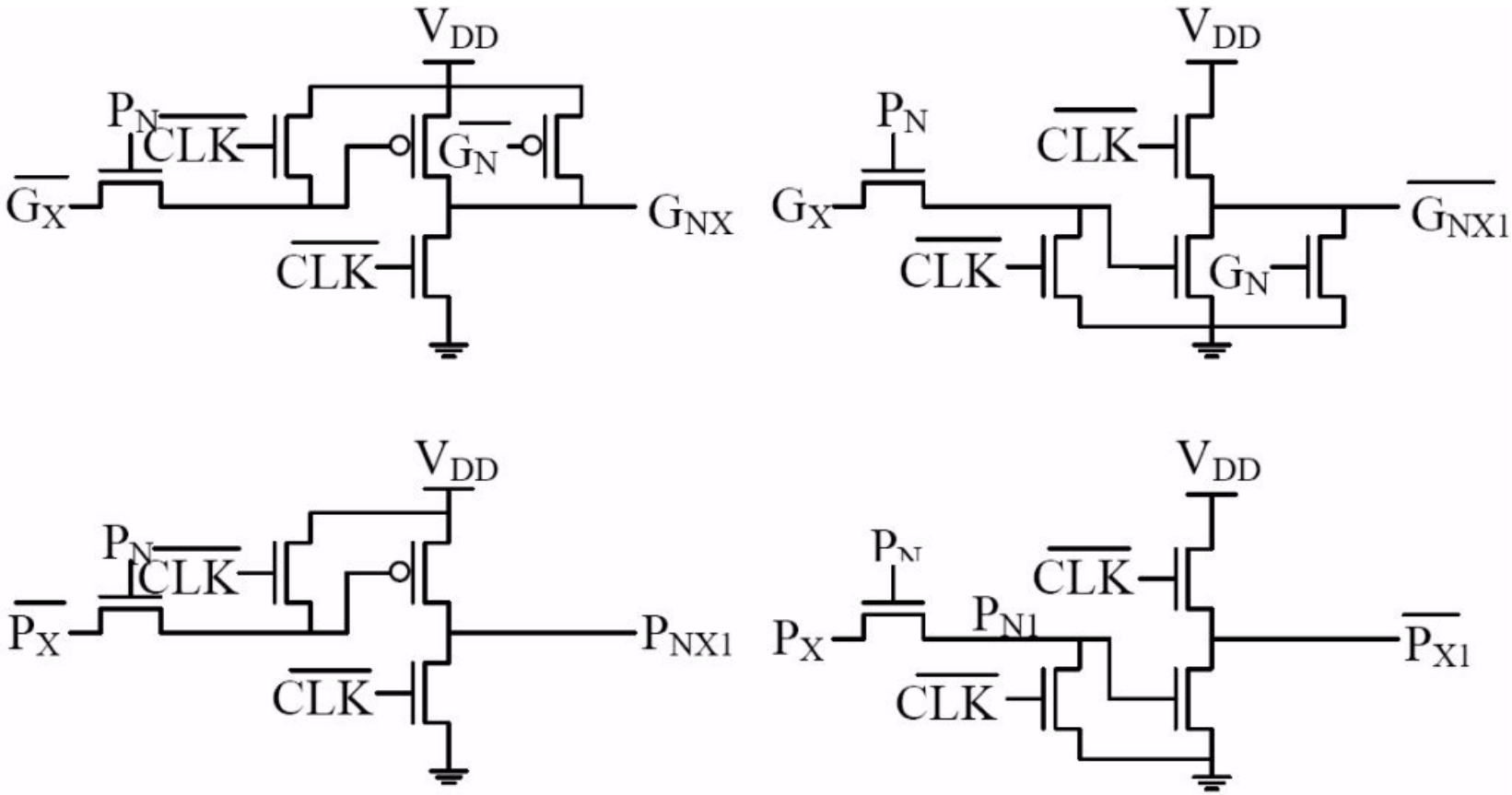
32-bit Tree Adder



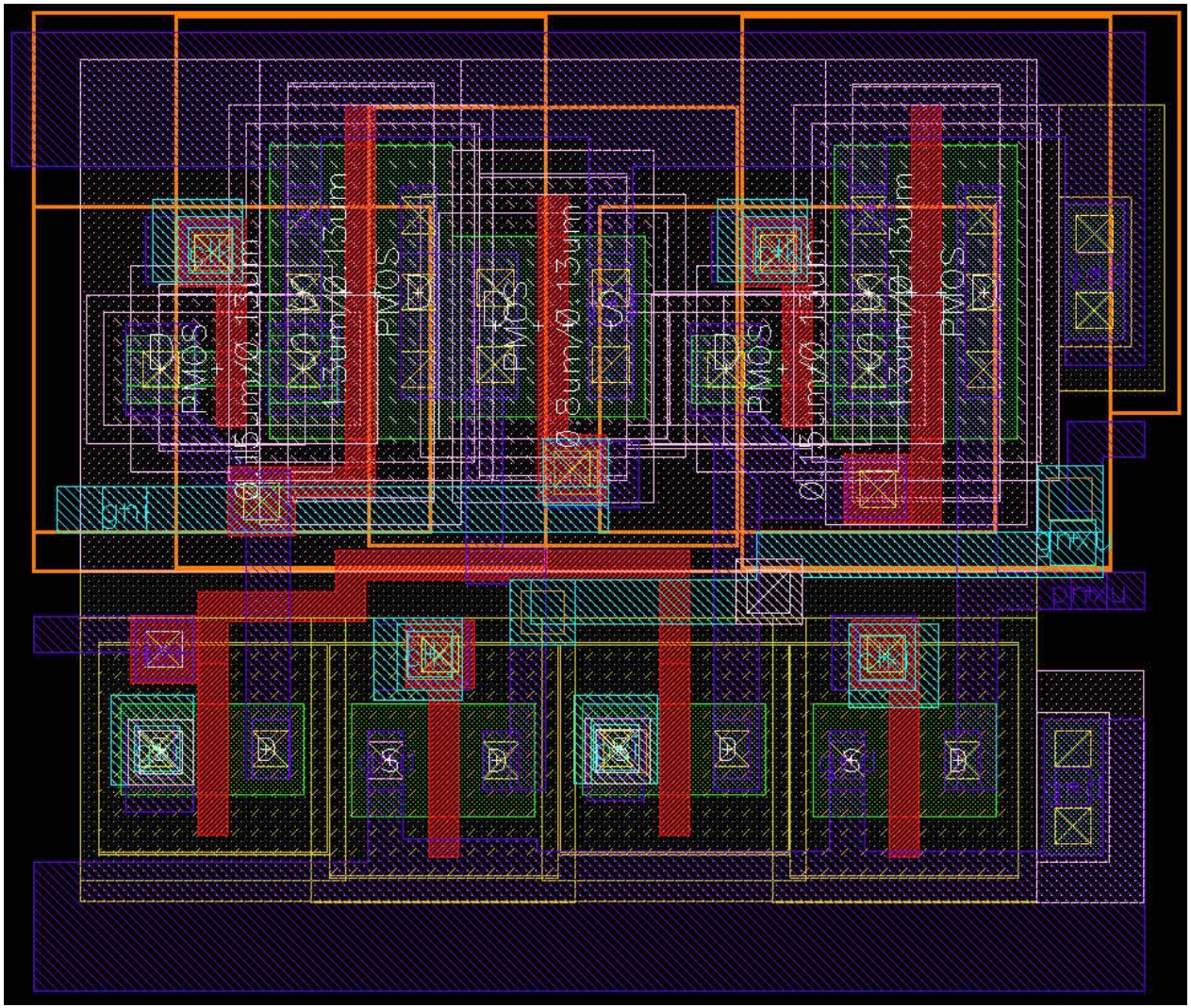
Layout of Two 130-nm 32-b Adders



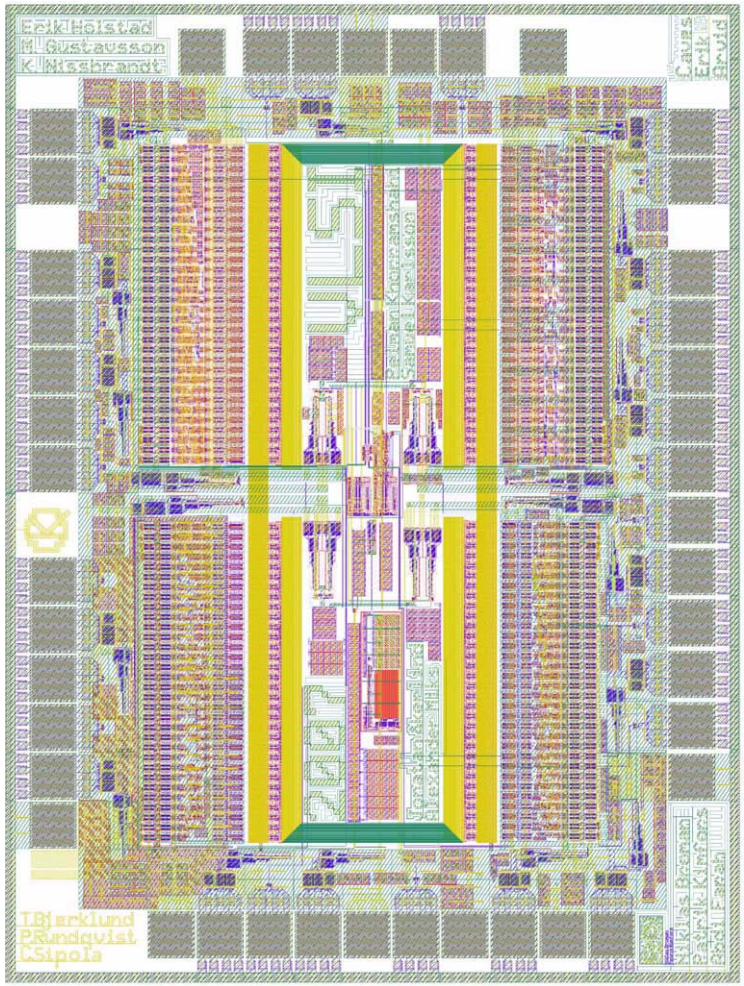
Dot Operator Circuits



130-nm Dot Operator Layout



ONE CHALMERS STUDENT CHIP



Another Chalmers Student Chip