Networks of Elastic Circuits

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Synchronous *elastic circuits* (also known as *latency-insensitive* and *latency-tolerant*) behave independently of the latencies of computations and communication channels. For example, the three sequences

$$X = \langle 1, *, *, 2, *, 5, 3, \ldots\rangle \quad Y = \langle 2, *, 0, *, 1, *, 4, \ldots\rangle \quad Z = \langle *, 3, *, 2, *, *, 6, *, 7, \ldots\rangle$$

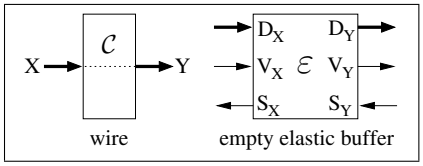
are an acceptable behavior of an elastic adder with input channels X, Y and output channel Z, where the absence of transfer on a particular channel at a given cycle is indicated by $*$. Indeed, the associated transfer subsequences (delete the $*$'s) make up a behavior of an ordinary (non-elastic) adder:

$$X' = \langle 1, 2, 5, 3, \ldots\rangle \quad Y' = \langle 2, 0, 1, 4, \ldots\rangle \quad Z' = \langle 3, 2, 6, 7, \ldots\rangle$$

Current interest in elasticity is motivated by the difficulties with timing and communication in large synchronous designs in nanoscale technologies [1]. Elastic circuits promise novel methods for microarchitectural design that can use variable latency components and tolerate static and dynamic changes in communication latencies, while still employing standard synchronous design tools and methods. At Intel, there is an extensive investigation of hardware design based on a specific elastic protocol, called SELF (Synchronous Elastic Flow)[2]. Our aim here is to present theoretical foundations of SELF.

Every elastic circuit $\mathcal{E}$ implements the behavior of an associated standard (non-elastic) circuit $\mathcal{C}$, as in the adder example above. For each wire X of $\mathcal{C}$, there are three in $\mathcal{E}$: the *data* wire D_X, and the single-bit control wires V_X and S_X (*valid* and *stop*). This triple of wires is a *channel* of $\mathcal{E}$. A transfer along the channel occurs when $V_X = 1$ and $S_X = 0$, thus requiring cooperation of the producer and the consumer.

As an example, the figure shows the interface of an empty elastic buffer—an elastic implementation of the wire. (Elastic buffers are fifos that follow the SELF protocol, and are crucial components of elastic design.)



Our main result states that (under favorable circumstances) "the network of elasticizations is an elasticization of the given network": if we have elastic circuits $\mathcal{E}_1, \ldots, \mathcal{E}_n$ implementing standard circuits $\mathcal{C}_1, \ldots, \mathcal{C}_n$ and if $\mathcal{C}$ is a standard network obtained by connecting some wires of the circuits $\mathcal{C}_i$, then connecting the corresponding channels (wire triples) of the elastic circuits $\mathcal{E}_i$ will produce a new elastic circuit which implements $\mathcal{C}$. As a special case, we prove the characteristic property of elastic circuits: plugging an empty elastic buffer in a channel of an elastic network produces an equivalent elastic network.

Adopting the standard framework in which circuits are modeled as stream transformers, we have developed a theory of elastic circuits with full mathematical rigor. Coming up with a useful definition of the intuitive concept of *elastic circuit* was a serious challenge. One needs to postulate liveness conditions just strong enough to guarantee that the elastic circuit will produce infinite transfer on the output wires in any friendly ("elastic") environment. Simple conditions for justifying the elastic feedback construction required some effort to find too, but we resolved the issue with an appropriate Combinational Loop Theorem.

References

[1] L. Carloni, K.L. McMillan, and A.L. Sangiovanni-Vincentelli. Theory of latency-insensitive design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, 20(9):1059–1076, September 2001.

[2] J. Cortadella, M. Kishinevsky, and B. Grundmann. SELF: Specification and design of a synchronous elastic architecture for DSM systems. Available at `www.lsi.upc.edu/~jordicf/gavina/BIB/files/self_tr.pdf`. Submitted for publication, 2005.

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