Designing Correct Circuits

Vienna, Austria, 25–26 March 2006

Call for Abstracts

We plan to hold a two-day workshop on the topic *Designing Correct Circuits*. The workshop will be held on 25–26 March 2004 in Vienna—just before ETAPS, the group of conferences that includes TACAS. The workshop will bring together researchers in formal methods for hardware design and verification from academia and industry. Much research in hardware verification now takes place in industry, as well as in academia. For the long term survival of our field, we must ensure that academics and industrial researchers continue to work together on the real problems facing microprocessor developers and those developing System on a Chip solutions. A major aim of this workshop is to open the necessary communication channels. This call invites you to submit a one page description of a talk that you would like to give at this workshop.

In recent years, formal methods have been used increasingly in the verification of large-scale circuit designs, particularly in the microprocessor industry. Great progress has been made in adapting and scaling up methods developed in academia, and in developing new methods to solve real verification problems. But more needs to be done. There are indications that we need to incorporate formal verification earlier in the design process, and this means thinking hard about our design and specification notations, and about how best to guide the verification process. We need to think about how to raise the level of abstraction at which we do verification. At the same time, it is becoming clear that non-functional properties like timing and power consumption must be taken into account early in the design process. This poses many interesting questions.

The aim of the workshop is to present the state of the art in hardware design and verification methods (from both an academic and an industrial viewpoint). Then, we hope to start a discussion on the question of what needs to be done next in research if we are to solve the huge problems facing both microprocessor manufacturers and the System on a Chip industry. The DCC workshops held in 2002 and 2004 (and earlier) were a great success; we hope for something similar in 2006.

Abstracts due by 12 November 2005

If you would like to speak at this workshop, submit a one page abstract of your talk to Mary Sheeran (ms@cs.chalmers.se) by 12 November 2005. The abstract should describe original work, and should indicate what distinguishes your work from other research on methods and languages for design and verification of hardware. Describe

the status of your work (for example industrial experience with conclusions, new idea with prototype implementation, new theory, comparison of methods). Please make clear how your talk will contribute to the kind of debate that we are hoping to generate. Include a list of references on a second page if you wish. Researchers from both industry and academia are encouraged to submit talks. Speakers from industry who would be willing to present research problems that they face (and with which they need help) would also be welcome. We would like to be able to present a broad view of the current state of the art in design and verification methods.

The final programme will be agreed by the workshop committee no later than 17 December 2005. A final version of material for the participants' proceedings will be due on 1 February 2006. This would preferably be a draft paper, but could also be slides. The workshop speakers and the workshop committee will decide after the workshop whether or not to make a more permanent record, for example by arranging a special issue of a journal.

Workshop Committee for DCC 2006

Dominique Borrione (TIMA Grenoble, France)
Elena Dubrova (KTH, Sweden)
Niklas Eén (Cadence Design Systems, USA)
Warren Hunt (UT Austin, USA)
Robert Jones (Intel Corporation, USA)
Wolfgang Kunz (TU Kaiserslautern, Germany)
Per Larsson-Edefors (Chalmers, Sweden)
Andrew Martin (IBM Research, USA)
Tom Melham (Oxford University, UK)
Johan Mårtensson (Jasper Design Automation, Sweden)
John O'Leary (Intel Corporation, USA)
Carl Pixley (Synopsys, USA)
Mary Sheeran (Chalmers, Sweden)
Satnam Singh (Microsoft Corporation, USA)
Joe Stoy (Bluespec, USA)
Jean Vuillemin (École Normale Supérieure, France)

Web Pages

The DCC'06 web page is at www.cs.chalmers.se/~ms/DCC06/.

The ETAPS'06 web page is at www.complang.tuwien.ac.at/etaps06/.

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Tom Melham (melham@comlab.ox.ac.uk)