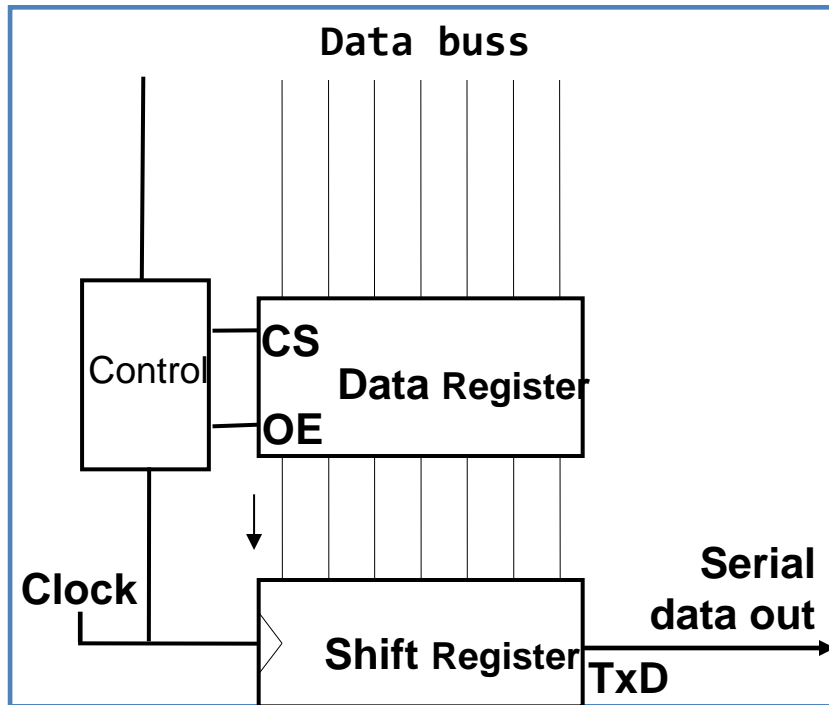




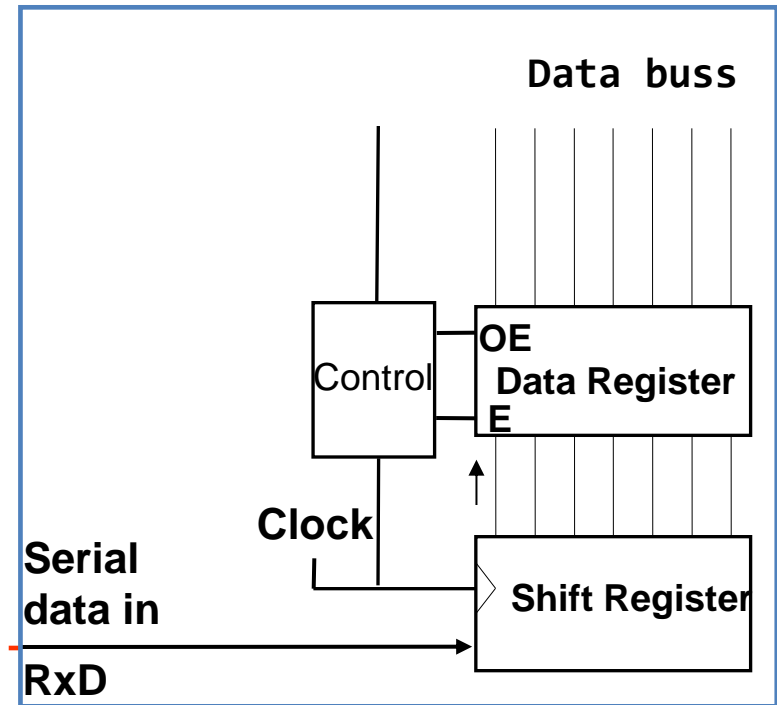
Seriekommunikation

Viktor Kämpe

Sändare



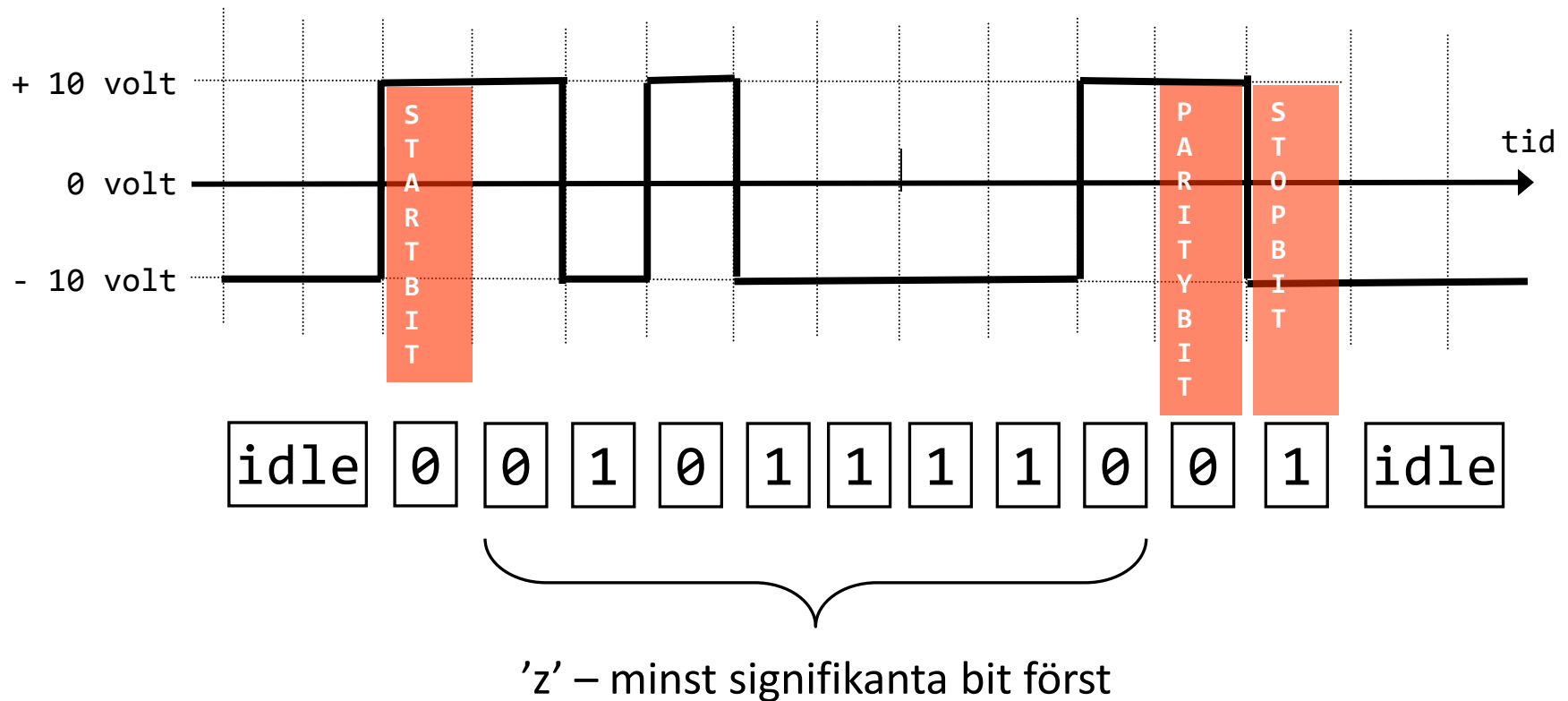
Mottagare



Sändare och mottagares klockor går i samma takt

RS232 – överföring av tecknet 'z'

tecknet "z" representeras av bitmönstret "0111 1010" (ASCII-tecken).



Gränssnitt

Serial Communication Interface (SCI)											
Offset		7	6	5	4	3	2	1	0	Mnemonic	Namn
\$00	R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCIBDH	Baud Rate Register High
	W										
\$01	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCIBDL	Baud Rate Register Low
	W										
\$02	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT	SCICR1	Control Register 1
	W										
\$03	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCICR2	Control Register 2
	W										
\$04	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCISR1	Status Register 1
	W										
\$05	R	0	0	0	0	0	BRK13	TXDIR	RAF	SCISR2	Status Register 2
	W										
\$06	R	R8	T8	0	0	0	0	0	0	SCIDRH	Data Register High
	W										
\$07	R	R7	R6	R5	R4	R3	R2	R1	R0	SCIDRL	Data Register Low
	W	T7	T6	T5	T4	T3	T2	T1	T0		

Recieve

Transmit

Init

Förkortningar

Serial Communication Interface (SCI)											
Offset		7	6	5	4	3	2	1	0	Mnemonic	Namn
\$00	R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCIBDH	Baud Rate Register High
	W										
\$01	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCIBDL	Baud Rate Register Low
	W										
\$02	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT	SCICR1	Control Register 1
	W										
\$03	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCICR2	Control Register 2
	W										
\$04	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCISR1	Status Register 1
	W										
\$05	R	0	0	0	0	0	BRK13	TXDIR	RAF	SCISR2	Status Register 2
	W										
\$06	R	R8	T8	0	0	0	0	0	0	SCIDRH	Data Register High
	W										
\$07	R	R7	R6	R5	R4	R3	R2	R1	R0	SCIDRL	Data Register Low
	W	T7	T6	T5	T4	T3	T2	T1	T0		

- SBR Serial Baud Rate
- TE / RE Transmit Enable / Recieve Enable
- TDRE Transmit Data Register Empty
- RDRF Recieve Data Register Full

Initiering

Serial Communication Interface (SCI)										Mnemonic	Namn
Offset		7	6	5	4	3	2	1	0		
\$00	R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCIBDH	Baud Rate Register High
	W										
\$01	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCIBDL	Baud Rate Register Low
	W										
\$02	R	LOOPS	SCISMAI	RSRC	M	WAKE	ILT	PE	PT	SCICR1	Control Register 1
	W										
\$03	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCICR2	Control Register 2
	W										
\$04	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCISR1	Status Register 1
	W										
\$05	R	0	0	0	0	0	BRK13	TXDIR	RAF	SCISR2	Status Register 2
	W										
\$06	R	R8	T8	0	0	0	0	0	0	SCIDRH	Data Register High
	W										
\$07	R	R7	R6	R5	R4	R3	R2	R1	R0	SCIDRL	Data Register Low
	W	T7	T6	T5	T4	T3	T2	T1	T0		



Recieve

1 Kolla om redo

2 Läs



Transmit

1 Kolla om redo

2 Skriv



Init

1 Sätt hastighet

2 Aktivera T och R

Skicka

Serial Communication Interface (SCI)											
Offset		7	6	5	4	3	2	1	0	Mnemonic	Namn
\$00	R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCIBDH	Baud Rate Register High
	W										
\$01	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCIBDL	Baud Rate Register Low
	W										
\$02	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT	SCICR1	Control Register 1
	W										
\$03	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCICR2	Control Register 2
	W										
\$04	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCISR1	Status Register 1
	W										
\$05	R	0	0	0	0	0	BRK13	TXDIR	RAF	SCISR2	Status Register 2
	W										
\$06	R	R8	T8	0	0	0	0	0	0	SCIDRH	Data Register High
	W										
\$07	R	R7	R6	R5	R4	R3	R2	R1	R0	SCIDRL	Data Register Low
	W	T7	T6	T5	T4	T3	T2	T1	T0		



Recieve

1 Kolla om redo

2 Läs



Transmit

1 Kolla om redo

2 Skriv



Init

1 Sätt hastighet

2 Aktivera T och R

Ta emot

Serial Communication Interface (SCI)											
Offset		7	6	5	4	3	2	1	0	Mnemonic	Namn
\$00	R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8	SCIBDH	Baud Rate Register High
	W										
\$01	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCIBDL	Baud Rate Register Low
	W										
\$02	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT	SCICR1	Control Register 1
	W										
\$03	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCICR2	Control Register 2
	W										
\$04	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCISR1	Status Register 1
	W										
\$05	R	0	0	0	0	0	BRK13	TXDIR	RAF	SCISR2	Status Register 2
	W										
\$06	R	R8	T8	0	0	0	0	0	0	SCIDRH	Data Register High
	W										
\$07	R	R7	R6	R5	R4	R3	R2	R1	R0	SCIDRL	Data Register Low
	W	T7	T6	T5	T4	T3	T2	T1	T0		



Recieve

1 Kolla om redo

2 Läs



Transmit

1 Kolla om redo

2 Skriv



Init

1 Sätt hastighet

2 Aktivera T och R



[Exempel i XCC12]

Förbättringar

- Byt busy-wait mot avbrottsdrivning